10-10-00

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Attorney Docket No. SEL 219

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION TRANSMITTAL LETTER

Transmitted herewith for filing is the patent application of:

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2. Title: Display Device

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Enclosed are:

X	17	Sheets of Drawings
		Formal
	X	Informal
X		Assignment of invention to Semiconductor Energy Laboratory Co., Ltd.
X	26	Pages of Specification
X	4	Pages of Claims
X		Abstract of The Disclosure
		Statement of Small Entity
X		Declaration and Power of Attorney
X		Information Disclosure Statement
X		Appointment of Associate Attorneys

Applicant claims priority under 35 USC §119 to the following foreign application:

Serial no. 11-287583 filed October 8, 1999 in Japan.

__X__ A certified copy of this priority document is enclosed herewith.

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Claims as Filed

	Number Filed		Number Extra	Rate	Fee
Total	23	-20	3	(small entity) x 9 (others) x 18	$54.00
Independent	5	-3	2	(small entity) x 40 (others) x 80	$160.00
Multiple Dependent	No			(small entity) x 135 (others) x 270	$0.00
Basic Fee				(small entity) x 355 (others) x 710	$710.00
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DISPLAY DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a display device, specifically, to an active matrix display device.

2. Description of the Related Art

A rapid development has been made lately in a technique of manufacturing an electronic device, a thin film transistor (TFT), for example, in which a semiconductor thin film is formed on an inexpensive glass substrate. This is because there is an increasing demand for an active matrix liquid crystal panel.

The active matrix liquid crystal panel has a pixel portion in which several hundred thousands to several millions of TFTs are arranged in a matrix-like manner, and displays an image by controlling electric charges flowing in and out a pixel electrodes connected to each of the TFTs by means of switching function of the TFTs.

Conventionally, thin film transistors arranged in the pixel portion are fabricated using amorphous silicon that is formed on a glass substrate.

However, recent years have found a thin film transistor being formed from a polycrystalline silicon film while using quarts for a substrate. In this case, peripheral driver circuits are integrated with the pixel portion so that both the circuits and the pixel portion are formed on the quartz substrate.

There is also known a technique in which a thin film transistor is fabricated from a crystalline silicon film formed on a glass substrate by using laser annealing or other technologies.

What comes to draw attention recently, in addition to a large size active matrix liquid crystal panel used as a display device of a personal computer, is a small one that is to be used in a front projector, a rear projector, and an HMD (head mount display). Smaller is better for the small size active matrix liquid crystal panel used for these electronic devices, and now a panel sized about 0.7 inch, diagonally, has been set on mass production line.

Referring to Fig. 17, the structure of a conventional active matrix liquid crystal panel is shown schematically. In Fig. 17, reference numeral 11000 denotes a liquid crystal panel, 11100, a source driver, 11200, a gate driver, 11300, a pixel portion, and 11400, an FPC terminal. The FPC terminal is a terminal for inputting video data, a clock signal, a power supply, etc. to the liquid crystal panel. When the lateral length of the pixel portion is given as W and the longitudinal length thereof as H, W/H is generally 4/3 or 16/9.

Accompanying with the recent demand for downsizing, however, it is no longer uncommon cases that constructing the device in accordance with the circuit layout shown in Fig. 17 is impossible. For instance, in some liquid crystal panel, the size of its substrate has to be reduced in the longitudinal direction of the gate driver. In this case, the area the source driver occupies causes a problem. That is, the number of elements constituting the source driver is greater as compared with the gate driver, and accordingly the source driver occupies a larger area. The conventional circuit layout can not deal with the downsizing because of this large occupied area of the source driver.

SUMMARY OF THE INVENTION

The present invention has been made in view of the above problem, and an object of the present invention is therefore to meet the demand for downsizing liquid crystal panels.

In a liquid crystal display device of the present invention, if the longitudinal length

of a pixel portion is given as W, the lateral length thereof as L, and the number of pixels in the pixel portion as **m** (length) x **n** (width), L > W and **m** < **n** are both satisfied, and a gate driver is placed above the pixel portion whereas a source driver is set on one side of the pixel portion. Video data inputted from the external are rearranged and then inputted to the source driver.

The structure of the present invention will be described below.

According to the present invention, there is provided a liquid crystal display device comprising:

a pixel portion including **m** x **n** pixels (**m** and **n** are both natural numbers and satisfy the relation **m** < **n**), the pixels each having a TFT;

a gate driver for feeding **n** gate signal lines with selection signals;

a source driver for feeding **m** source signal lines with video data; and

a video data converter circuit, characterized in that

the video data converter circuit converts first video data (**h**, **k**) (**h** = 1 ~ **m**, **k** = 1 ~ **n**) into second video data, and in that

the video data (**h**, **k**) constituting the first video data is converted into {**m**(**k** - 1) + **h**}-th video data that constitutes the second video data.

According to the present invention, there is provided a liquid crystal display device comprising:

a pixel portion including **m** x **n** pixels (in a pixel (**h**, **k**),**h** = 1 ~ **m**, **k** = 1 ~ **n**, with **m** and **n** both being natural numbers and satisfying the relation **m** < **n**), said pixels each having a TFT;

a gate driver for feeding **n** gate signal lines with selection signals;

a source driver for feeding **m** source signal lines with video data; and

a video data converter circuit, characterized in that

said video data converter circuit converts first video data (**h**, **k**) (**h** = 1 ~ **m**, **k** = 1 ~ **n**) which is to be fed to said pixel (**h**, **k**) into second video data, and in that

the video data (**h**, **k**) constituting the first video data is converted into {**m**(**k** - 1) + **h**}-th video data that constitutes the second video data.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Fig. 1 is a schematic structural diagram showing a liquid crystal display device according to the present invention;

Fig. 2 is a circuit structural diagram showing a liquid crystal panel of the liquid crystal display device according to the present invention;

Fig. 3 is a chart illustrating the operation of converting video data (VIDEO) by a video data converter circuit according to the present invention;

Fig. 4 is a diagram showing an example of the circuit structure of the video data converter circuit according to the present invention;

Fig. 5 is a circuit structural diagram showing a liquid crystal panel of a liquid crystal display device according to the present invention;

Fig. 6 is a chart illustrating the operation of converting video data (VIDEO) by a video data converter circuit according to the present invention;

Fig. 7 is a circuit structural diagram showing a liquid crystal panel of a liquid crystal display device according to the present invention;

Figs. 8A to 8D are diagrams showing an example of a process of manufacturing a liquid crystal panel of a liquid crystal display device according to the present invention;

Figs. 9A to 9D are diagrams showing the exemplary process of manufacturing the

liquid crystal panel of the liquid crystal display device according to the present invention;

Figs. 10A to 10D are diagrams showing the exemplary process of manufacturing the liquid crystal panel of the liquid crystal display device according to the present invention;

Figs. 11A and 11B are diagrams showing the exemplary process of manufacturing the liquid crystal panel of the liquid crystal display device according to the present invention;

Fig. 12 is a diagram showing the exemplary process of manufacturing the liquid crystal panel of the liquid crystal display device according to the present invention;

Fig. 13 is a graph showing an applied voltage - transmittance characteristic of a ferroelectric liquid crystal that exhibits a Half-V shape type electro optical characteristic;

Figs. 14A and 14B are diagrams showing examples of electronic equipment having incorporated therein a liquid crystal display device of the present invention;

Figs. 15A to 15F are diagrams showing examples of electronic equipment having incorporated therein one or more liquid crystal display devices of the present invention;

Fig. 16 is a chart illustrating the operation of converting video data (VIDEO) by a video data converter circuit according to the present invention; and

Fig. 17 is a schematic structural diagram showing a liquid crystal panel of prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A liquid crystal display device according to an embodiment mode of the present invention is shown in Fig. 1.

The liquid crystal display device of this embodiment mode, shown in Fig. 1, has a liquid crystal panel 1000 and a video data converter circuit 2000. The liquid crystal panel 1000 includes a gate driver 1100, a source driver 1200, a pixel portion 1300, and an FPC terminal

1400. The video data converter circuit 2000 receives video data (VIDEO) inputted thereto. The inputted video data (VIDEO) is converted into video data n (VIDEOn) by the video data converter circuit 2000, and then the video data converter circuit 2000 outputs the video data n (VIDEOn) to the source driver 1200 of the liquid crystal panel 1000. The index "n" in the video data n stands for "new". Note that, although this embodiment mode describes the liquid crystal display device of the present invention taking as an example a liquid crystal panel with a pixel portion having 5 (width) x 4 (length) pixels, the liquid crystal display device of the present invention is not limited thereto.

In the liquid crystal display panel of the liquid crystal display device according to the present invention, **a** > **b** with the lateral length of the liquid crystal panel 1000 (the length of the liquid crystal panel in the longitudinal direction of the gate driver) being **a,** and the longitudinal length of the liquid crystal panel 1000 (the length of the liquid crystal panel in the longitudinal direction of the source driver) being **b.** Also, if the lateral length of the pixel portion 1300 (the length of the pixel portion 1300 in the longitudinal direction of the gate driver) is given as W while the longitudinal length of the pixel portion 1300 (the length of the pixel portion 1300 in the longitudinal direction of the source driver) is given as H, the relation W > H should be satisfied.

Referring now to Fig. 2, the outline of the circuit structure of the liquid crystal panel of the liquid crystal display device according to the present invention will be explained. Fig. 2 shows the circuit structure of the pixel portion 1300. The pixel portion 1300 is structured such that pixels 1310 are arranged in a matrix-like manner. Each of the pixels 1310 has a TFT 1320, a holding capacitor 1330, and a liquid crystal 1340. A pixel electrode (not shown) connected to either one end of a source of the TFT or of a drain of the TFT and an opposite electrode (not shown) cooperate to apply voltage to the liquid crystal. The opposite electrode is connected to a common electric potential (COM). The holding capacitor 1330 may not exactly be as shown

in Fig. 2. The pixels 1310 constituting the pixel portion 1300 are respectively denoted by symbols (1, 1), (1, 2), ····· and (4, 5). The respective pixels are from now on referred to by their symbols, as in "pixel (1, 1)".

The gate driver 1100 sequentially feeds selection signals to gate signal lines G1, G2, G3, G4, and G5. The gate signal line G1 is connected to a gate electrode of the TFT 1320 of each of the pixel (1, 1), the pixel (2, 1), the pixel (3, 1), and the pixel (4, 1). The gate signal line G2 is connected to a gate electrode of the TFT 1320 of each of the pixel (1, 2), the pixel (2, 2), the pixel (3, 2), and the pixel (4, 2). The gate signal line G3 is connected to a gate electrode of the TFT 1320 of each of the pixel (1, 3), the pixel (2, 3), the pixel (3, 3), and the pixel (4, 3). The gate signal line G4 is connected to a gate electrode of the TFT 1320 of each of the pixel (1, 4), the pixel (2, 4), the pixel (3, 4), and the pixel (4, 4). The gate signal line G5 is connected to a gate electrode of the TFT 1320 of each of the pixel (1, 5), the pixel (2, 5), the pixel (3, 5), and the pixel (4, 5).

Inputted to the source driver 1200 is the video data n (VIDEOn) created in the video data converter circuit 2000. The source driver 1200 feeds video data to source electrodes of the TFTs of the pixels through source signal lines S1, S2, S3, and S4, respectively. The source signal line S1 is connected to a source region of the TFT of each of the pixel (1, 1), the pixel (1, 2), the pixel (1, 3), the pixel (1, 4), and the pixel (1, 5). The source signal line S2 is connected to a source region of the TFT of each of the pixel (2, 1), the pixel (2, 2), the pixel (2, 3), the pixel (2, 4), and the pixel (2, 5). The source signal line S3 is connected to a source region of the TFT of each of the pixel (3, 1), the pixel (3, 2), the pixel (3, 3), the pixel (3, 4), and the pixel (3, 5). The source signal line S4 is connected to a source region of the TFT of each of the pixel (4, 1), the pixel (4, 2), the pixel (4, 3), the pixel (4, 4), and the pixel (4, 5).

The function of the video data converter circuit 2000 and the operation thereof will

be described next. The video data converter circuit 2000 converts video data (VIDEO) into video data n (VIDEOn). Referring to Fig. 3, the drawing illustrates how the video data (VIDEO) is converted into the video data n (VIDEOn). Each video data in the video data (VIDEO) has its own symbol such as (1, 1), (1, 2), ····· and (4, 5). The respective video data are from now on referred to by their symbols, as in "video data (1, 1)".

The symbols allotted to the video data correspond to the symbols that designate the pixels. That is, the video data (1, 1) is fed to the pixel (1, 1)(to the source region of the TFT of the pixel (1, 1), to be strict), and the video data (1, 2) is fed to the pixel (1, 2).

The video data (VIDEO) before conversion consists of the video data (1, 1), the video data (1, 2), the video data (1, 3), ·····, the video data (4, 4), and the video data (4, 5) which are arranged in this order. In the liquid crystal panel 1000 of the liquid crystal display device according to the present invention, however, the pixel (1, 1) is the first to be fed with the video data, the pixel (2, 1) is the second, and then the pixel (3, 1), the pixel (4, 1), the pixel (1, 2), ·····, the pixel (3, 5), and the pixel (4, 5) is the last. Therefore, the video data cannot be inputted to proper pixels as long as they constitute the video data (VIDEO) while being arranged in the before-conversion order.

The before-conversion video data (VIDEO) thus needs to be converted into video data n (VIDEOn) by the video data converter circuit 2000. The after-conversion video data n (VIDEOn) consists of the video data (1, 1), the video data (2, 1), the video data (3, 1), ·····, the video data (3, 5), and the video data (4, 5) which are arranged in this order. Now the respective video data can be inputted to proper pixels.

Described next is the circuit structure of the video data converter circuit 2000 according to this embodiment mode, with the circuit structure schematically shown in Fig. 4. In this embodiment mode, the video data converter circuit 2000 has a video formatter 2100, a

memory 2200, and an address generator 2300. The video data (VIDEO) is inputted to the video formatter 2100 of the video converter circuit 2000, and the video data in the video data (VIDEO) are sequentially stored in the memory 2200. The address generator 2300 gives an address to each video data so that the video data stored in the memory 2200 are read out in the predetermined order, and the generator controls the transmission of video signals from the memory 2200 to the video formatter 2100. The video data n (VIDEOn) is then outputted from the video formatter 2100.

Both the video data (VIDEO) and the video data n (VIDEOn) are digital data in this embodiment mode. However, the present invention can handle inputting and outputting analog video data by employing a D/A converter circuit and an A/D converter circuit.

Reference is made to Fig. 5 where a liquid crystal panel of the liquid crystal display device according to the present invention is shown. This liquid crystal panel has a pixel portion including m (length) x n (width) pixels. The numerals expressed as m and n are both natural numbers. Each pixel has its own symbol and is referred to as pixel (h, k) (h = 1 ~ m, k = 1 ~ n).

A gate driver 3100 sequentially feeds selection signals to gate signal lines G1, G2, ·····, Gn - 1, and Gn. The gate signal line G1 is connected to a gate electrode of a TFT 3320 of each of the pixel (1, 1), the pixel (2, 1), ·····, the pixel (m - 1, 1) and the pixel (m, 1). The gate signal line G2 is connected to a gate electrode of the TFT 3320 of each of the pixel (1, 2), the pixel (2, 2), ·····, the pixel (m - 1, 2) and the pixel (m, 2). In a similar manner, the gate signal line Gn is connected to a gate electrode of the TFT 3320 of each of the pixel (1, n), the pixel (2, n), ·····, the pixel (m - 1, n) and the pixel (m, n).

Inputted to a source driver 3200 is video data n (VIDEOn) created in the video data converter circuit. The source driver 3200 feeds video data to source electrodes of the TFTs of the pixels through source signal lines S1, S2, ·····, Sm - 1, and Sm, respectively. The source signal

line S1 is connected to a source region of the TFT 3320 of each of the pixel (1, 1), the pixel (1, 2), ·····, the pixel (1, n - 1), and the pixel (1, n). The source signal line S2 is connected to a source region of the TFT 3320 of each of the pixel (2, 1), the pixel (2, 2), ·····, the pixel (2, n - 1), and the pixel (2, n). In a similar manner, the source signal line Sm is connected to a source region of the TFT 3320 of each of the pixel (m, 1), the pixel (m, 2), ·····, the pixel (m, n - 1), and the pixel (m, n).

The description given next is about the making of the video data (VIDEOn) to be inputted to the liquid crystal panel of the present invention which is shown in Fig. 5.

Referring to Fig. 6, the video data (VIDEO) before inputted to the video converter circuit (before conversion) consists of the video data (1, 1), the video data (1, 2), ·····, the video data (1, n - 1), the video data (1, n), the video data (2, 1), the video data (2, 2), ·····, the video data (m, 1), the video data (m, 2), ·····, the video data (m, n - 1), and the video data (m, n), which are arranged in this order.

The before-conversion video data (VIDEO) is converted into video data n (VIDEOn) by the video data converter circuit. The after-conversion video data n (VIDEOn) consists of the video data (1, 1), the video data (2, 1), ·····, the video data (m - 1, 1), the video data (m, 1), the video data (1, 2), ·····, the video data (m, n - 1), the video data (1, n), the video data (2, n), ·····, the video data (m - 1, n), and the video data (m, n) which are arranged in this order. The respective video data thus can be inputted to proper pixels.

Therefore, in the liquid crystal display panel of this embodiment mode, the video data (h, k) of the video data (VIDEO) corresponds to the {m(k - 1) + h}-th data among the data that constitute the video data n (VIDEOn).

For example, the video data (1, 1) of the video data (VIDEO) corresponds to the first video data among the data that constitute the video data n (VIDEOn). The video data (2, 2) of

the video data (VIDEO) corresponds to the (m + 2)-th video data among the data that constitute the video data n (VIDEOn). The video data (m, n) of the video data (VIDEO) corresponds to the (m x n)-th video data among the data that constitute the video data n (VIDEOn).

By controlling the address generator of the video data converter circuit in this way, the video data are read out of the memory in the appropriate order and inputted to the liquid crystal panel. An image as desired can thus be obtained.

Referring next to Fig. 7, another liquid crystal panel according to this embodiment mode is shown. The liquid crystal panel in Fig. 7 has a source driver on each of its left side and right side.

A source driver 4200 feeds video data to the odd-numbered source signal lines S1 and S3, whereas a source driver 4300 feeds video data to the even-numbered signal lines S2 and S4.

This arrangement makes it possible to apply the present invention even if the circuit structure of the source driver is complicated and the area the source driver occupies is accordingly large.

In addition, left-right inversion of the display screen can readily be achieved by inverting the direction of the operation of the gate driver (the order to feed selection signals).

As shown in Fig. 16, when the video data (VIDEO) is converted by the video converter circuit, each video data is divided into four data to create VIDEOn1, VIDEOn2, VIDEOn3, and VIDEOn4. Shown here is an example in which the video data (VIDEO) is divided into four data, but the number of division is not limited to four.

[Embodiment 1]

This embodiment gives a description with reference to Figs. 8A to 12 on an example of a process of manufacturing a liquid crystal panel for a display device of the present invention.

In the liquid crystal panel in this embodiment, a pixel portion, a source driver, a gate driver, etc. are integrally formed on a single substrate. For conveniences sake in explanation, it is assumed that a pixel TFT, an N-channel TFT for forming an analog switch of a source driver (driver circuit), and a P-channel TFT and an N-channel TFT for forming an inverter circuit are formed on the same substrate in the drawings.

In Fig. 8A, a low-alkaline glass substrate or a quartz substrate can be used as a substrate 6001. In this embodiment, a low-alkaline glass substrate was used. In this case, a heat treatment at a temperature lower by about 10 to 20°C than the strain point of glass may be performed in advance. On the surface of this substrate 6001 on which TFTs are to be formed, a base film 6002 such as a silicon oxide film, a silicon nitride film or a silicon oxynitride film is formed in order to prevent the diffusion of impurities from the substrate 6001. For example, a laminate is formed from: a silicon oxynitride film which is fabricated from SiH_4, NH_3, and N_2O by plasma CVD into 100 nm thickness; and a silicon oxynitride film which is similarly fabricated from SiH_4 and N_2O into 200 nm.

Next, a semiconductor film 6003a that has an amorphous structure and a thickness of 20 to 150 nm (preferably, 30 to 80 nm) is formed by a known method such as plasma CVD or sputtering. In this embodiment, an amorphous silicon film is formed to a thickness of 54 nm by plasma CVD. As semiconductor films which have an amorphous structure, there are an amorphous semiconductor film and a microcrystalline semiconductor film; and a compound semiconductor film with an amorphous structure such as an amorphous silicon germanium film may also be applied. Further, the base film 6002 and the amorphous silicon film 6003a can be formed by the same deposition method, so that the two films can be formed in succession. By not exposing the base film to the atmospheric air after the formation of the base film, the surface of the base film can be prevented from being contaminated, as a result of which the dispersion

in characteristics of the fabricated TFTs and the variation in the threshold voltage thereof can be reduced. (Fig. 8A)

Then, by a known crystallization technique, a crystalline silicon film 6003b is formed from the amorphous silicon film 6003a. For example, a laser crystallization method or a thermal crystallization method (solid phase growth method) may be applied. Here, in accordance with the technique disclosed in Japanese Patent Application Laid-Open No. Hei 7-130652, the crystalline silicon film 6003b was formed by the crystallization method using a catalytic element. It is preferred that, prior to the crystallization step, heat treatment is carried out at 400 to 500°C for about one hour though it depends on the amount of hydrogen contained, so that, after the amount of hydrogen contained is reduced to 5 atomic% or less, the crystallization is carried out. The atoms are subjected to re-configuration to become dense when an amorphous silicon film is crystallized; and therefore, the thickness of the crystalline silicon film fabricated is reduced by about 1 to 15% than the initial thickness of the amorphous silicon film (54 nm in this embodiment). (Fig. 8B)

Then, the crystalline silicon film 6003b is patterned into islands, whereby island semiconductor layers 6004 to 6007 are formed. Thereafter, a mask layer 6008 of a silicon oxide film is formed to a thickness of 50 to 150 nm by plasma CVD or sputtering. (Fig. 8C) In this Embodiment the thickness of the mask layer 6008 is set at 130 nm.

Then, a resist mask 6009 is provided, and, into the entire surfaces of the island semiconductor layers 6004 to 6007 becoming the N-channel type TFTs, and boron (B) was added as an impurity element imparting p-type conductivity, at a concentration of about 1×10^{16} to 5×10^{17} atoms/cm^3. The addition of boron (B) here is performed for the purpose of threshold voltage control. The addition of boron (B) may be effected either by ion doping or it may be added

simultaneously when the amorphous silicon film is formed. The addition of boron (B) here was not always necessary. (Fig. 8D)

In order to form the LDD regions of the N-channel TFTs in the driver circuit such as the driver, an impurity element imparting n-type conductivity is selectively added to the island semiconductor layers 6010 to 6012. For this purpose, resist masks 6013 to 6016 were formed in advance. As the impurity element imparting the n-type conductivity, phosphorus (P) or arsenic (As) may be used; here, in order to add phosphorus (P), ion doping using phosphine (PH_3) was applied. The concentration of phosphorus (P) in the impurity regions 6017 and 6018 thus formed may be set within the range of from 2×10^{16} to 5×10^{19} atoms/cm^3. In this specification, the concentration of the impurity element contained in the thus formed impurity regions 6017 to 6019 imparting n-type conductivity is represented by (n^-). Further, the impurity region 6019 is a semiconductor layer for forming the storage capacitor of the pixel section; into this region, phosphorus (P) was also added in the same concentration. (Fig. 9A) Thereafter, resist masks 6013 to 6016 are removed.

Next, the mask layer 6008 is removed by hydrofluoric acid or the like, and the step of activating the impurity elements added in the steps shown in Figs. 8D and 9A is carried out. The activation can be carried out by performing heat treatment in a nitrogen atmosphere at 500 to 600°C for 1 to 4 hours or by using the laser activation method. Further, both methods may be jointly performed. In this embodiment, the laser activation method was employed, and a KrF excimer laser beam (with a wavelength of 248 nm) was used. In this embodiment, the shape of the laser light is formed into a linear beam, and the entire surface of the substrate on which island semiconductor layers are formed is scanned under the condition that the oscillation frequency was 5 to 50 Hz, the energy density was 100 to 500 mJ/cm^2, and the overlap ratio of the linear beam was 80 to 98%. Note that there is no item of the laser light irradiation condition that is subjected

to limitation, and they can be appropriately determined.

Then, a gate insulating film 6020 is formed from an insulating film comprising silicon to a thickness of 10 to 150 nm, by plasma CVD or sputtering. For example, a silicon oxynitride film is formed to a thickness of 120 nm. As the gate insulating film, another insulating film comprising silicon may be used as a single layer or a laminate structure. (Fig. 9B)

Next, in order to form a gate electrode, a first conductive layer is deposited. This first conductive layer may be comprised of a single layer but may also be comprised of a laminate consisting of two or three layers. In this embodiment, a conductive layer (A) 6021 comprising a conductive metal nitride film and a conductive layer (B) 6022 comprising a metal film are laminated. The conductive layer (B) 6022 may be formed of an element selected from the group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo) and tungsten (W) an alloy comprised mainly of the above-mentioned element, or an alloy film (typically, an Mo-W alloy film or an Mo-Ta alloy film) comprised of a combination of the above-mentioned elements, while the conductive layer (A) 6021 comprises tantalum nitride (TaN), tungsten nitride (WN), titanium nitride (TiN), or molybdenum nitride (MoN). Further, as the substitute materials of the conductive film (A) 6021, tungsten silicide, titanium silicide, or molybdenum silicide may also be applied. The conductive layer (B) 6022 may preferably have its impurity concentration reduced in order to decrease the resistance thereof; in particular, as for the oxygen concentration, the concentration may be set to 30 ppm or less. For example, tungsten (W) could result in realizing a resistivity of 20 $\mu\Omega$cm or less by rendering the oxygen concentration thereof to 30 ppm or less.

The conductive layer (A) 6021 may be set to 10 to 50 nm (preferably, 20 to 30 nm), and the conductive layer (B) 6022 may be set to 200 to 400 nm (preferably, 250 to 350 nm). In this embodiment, as the conductive layer (A) 6021, a tantalum nitride film with a thickness of 50 nm

was used, while, as the conductive layer (B) 6022, a Ta film with a thickness of 350 nm was used, both films being formed by sputtering. In case of performing sputtering here, if a suitable amount of Xe or Kr is added into the sputtering gas Ar, the internal stress of the film formed is alleviated, whereby the film can be prevented from peeling off. Though not shown, it is effective to form a silicon film, into which phosphorus (P) is doped, to a thickness of about 2 to 20 nm underneath the conductive layer (A) 6021. By doing so, the adhesiveness of the conductive film formed thereon can be enhanced, and at the same time, oxidation can be prevented. In addition, the alkali metal element slightly contained in the conductive film (A) or the conductive film (B) can be prevented from diffusing into the gate insulating film 6020. (Fig. 9C)

Next, resist masks 6023 to 6027 are formed, and the conductive layer (A) 6021 and the conductive layer (B) 6022 are etched together to form gate electrodes 6028 to 6031 and a capacitor wiring 6032. The gate electrodes 6028 to 6031 and the capacitor wiring 6032 are formed in such a manner that the layers 6028a to 6032a comprised of the conductive layer (A) and the layers 6028b to 6032b comprised of the conductive layer (B) are formed as one body respectively. In this case, the gate electrodes 6028 to 6030 formed for the driver circuit are formed so as to overlap the portions of the impurity regions 6017 and 6018 through the gate insulating film 6020. (Fig. 9D)

Then, in order to form the source region and the drain region of the P-channel TFT in the driver circuit, the step of adding an impurity element imparting p-type conductivity is carried out. Here, by using the gate electrode 6028 as a mask, impurity regions are formed in a self-alignment manner. In this case, the region in which the N-channel TFTs will be formed is covered with a resist mask 6033 in advance. Thus, impurity regions 6034 were formed by ion doping using diborane (B_2H_6). The concentration of boron (B) in this region is brought to 3×10^{20}

to 3 x 10^{21} atoms/cm^3. In this specification, the concentration of the impurity element imparting p-type contained in the impurity regions 6034 is represented by (p^{++}). (Fig. 10A)

Next, in the N-channel TFTs, impurity regions that function as source regions or drain regions were formed. Resist masks 6035 to 6037 were formed, and an impurity element for imparting the n-type conductivity was added to form impurity regions 6038 to 6042. This was carried out by ion doping using phosphine (PH_3), and the phosphorus (P) concentration in these regions was set within a region of 1 x 10^{20} to 1 x 10^{21} atoms/cm^3. In this specification, the concentration of the impurity element imparting the n-type contained in the impurity regions 6038 to 6042 formed here is represented by (n^+). (Fig. 10B)

In the impurity regions 6038 to 6042, the phosphorus (P) or boron (B) that are added in the preceding steps are contained, however, as compared with the impurity element concentration, phosphorus is added here at a sufficiently high concentration, so that the influence by the phosphorus (P) or boron (B) added in the preceding steps need not be taken into consideration. Further, the concentration of the phosphorus (P) that is added into the impurity regions 6038 is 1/2 to 1/3 of the concentration of the boron (B) added in the step shown in Fig. 10A; and thus, the p-type conductivity was secured, and no influence was exerted on the characteristics of the TFTs.

Then, the step of adding an impurity imparting n-type for formation of the LDD regions of the N-channel TFT in the pixel section was carried out. Here, by using the gate electrode 6031 as a mask, the impurity element for imparting n-type was added in a self-alignment manner. The concentration of phosphorus (P) added was 1 x 10^{16} to 5 x 10^{18} atoms/cm^3; by thus adding phosphorus at a concentration lower than the concentrations of the impurity elements added in the steps shown in Figs. 9A, 10A and 10B, only impurity regions 6043 and 6044 are substantially

formed. In this specification, the concentration of the impurity element imparting the n-type contained in the impurity regions 6043 and 6044 is represented by (n^-). (Fig. 10C)

Here, a film such as SiON film or the like may be formed into 200 nm thickness as an interlayer film for preventing peeling of gate electrode Ta.

Thereafter, in order to activate the impurity elements, which were added at their respective concentrations for imparting n-type or p-type, a heat treatment step is carried out. This step can be carried out by furnace annealing, laser annealing or rapid thermal annealing (RTA). Here, the activation step was performed by furnace annealing. Heat treatment is carried out in a nitrogen atmosphere with an oxygen concentration of 1 ppm or less, preferably 0.1 ppm or less, at 400 to 800°C, generally at 500 to 600°C; in this embodiment, the heat treatment was carried out at 500° C for 4 hours. Further, in case a substrate such as a quartz substrate which has heat resistance is used as the substrate 6001, the heat treatment may be carried out at 800°C for one hour; in this case, the activation of the impurity elements and the formation of junctions between the impurity regions into which the impurity element was added and the channel-forming region could be performed well. Note that in case that the above stated interlayer film for preventing peeling of gate electrode Ta is formed, there are cases that such effect cannot be obtained.

By this heat treatment, in the metal films 6028b to 6032b, which form the gate electrodes 6028 to 6031 and the capacitor wiring 6032, conductive layers (C) 6028c to 6032c are formed with a thickness of 5 to 80 nm as measured from the surface. For example, in the case the conductive layers (B) 6028b to 6032b are made of tungsten (W), tungsten nitride (WN) is formed; in the case of tantalum (Ta), tantalum nitride (TaN) can be formed. Further, the conductive layers (C) 6028c to 6032c can be similarly formed by exposing the gate electrodes 6028 to 6031 and the capacitor wiring 6032 to a plasma atmosphere containing nitrogen using nitrogen, ammonia or the like. Further, heat treatment was carried out in an atmosphere containing 3 to 100% of

hydrogen at 300 to 450°C for 1 to 12 hours, thus performing the step of hydrogenating the island semiconductor layers. This step is a step for terminating the dangling bonds of the semiconductor layers by the thermally excited hydrogen. As another means for the hydrogenation, plasma hydrogenation (using the hydrogen excited by plasma) may be performed.

In the case the island semiconductor layers were fabricated from an amorphous silicon film by the crystallization method using a catalytic element, a trace amount of the catalytic element remained in the island semiconductor layers. Of course, it is possible to complete the TFT even in such a state however, it was more preferable to remove the residual catalytic element at least from the channel-forming region. As one of the means for removing this catalytic element, there is the means utilizing the gettering function of phosphorus (P). The concentration of phosphorus (P) necessary to perform gettering is at the same level as that of the impurity region (n^+) which was formed in the step shown in Fig. 10B; by the heat treatment at the activation step carried out here, the catalytic element could be gettered from the channel-forming region of the N-channel and the P-channel TFTs. (Fig. 10D)

A first interlayer insulating film 6045 is formed of a silicon oxide film or a silicon oxynitride film with a thickness of 500 to 1500 nm, and contact holes reaching the source regions or the drain regions which are formed in the respective island semiconductor layers, are formed; and source wirings 6046 to 6049 and drain wirings 6050 to 6053 are formed. (Fig. 11A) Though not shown, in this embodiment, these electrodes were formed from a three-layer structure which was constituted by continuously forming a Ti film with a thickness of 100 nm, an aluminum film containing Ti and having a thickness of 500 nm, and a Ti film with a thickness of 150 nm by sputtering.

Next, as a passivation film 6054, a silicon nitride film, a silicon oxide film or a silicon oxynitride film is formed to a thickness of 50 to 500 nm (typically, 100 to 300 nm). In this

Embodiment the passivation film 6054 is made into a laminate film of a 50 nm thick silicon nitride film and a 24.5 nm silicon oxide film. In the case that a hydrogenating treatment is carried out in this state, a desirable result was obtained in respect of the enhancement in characteristics of the TFTs. For example, it is preferable to carry out heat treatment in an atmosphere containing 3 to 100% of hydrogen at 300 to 450° C for 1 to 12 hours; or, in the case that the plasma hydrogenation method is employed, a similar effect is obtained. Here, openings may be formed in the passivation film 6054 at the position at which contact hole for connecting the pixel electrodes and drain wirings will be formed later. (Fig. 11A)

Thereafter, a second interlayer insulating film 6055 comprised of an organic resin is formed to a thickness of 1.0 to 1.5 μm. As the organic resin, polyimide, acrylic, polyamide, polyimideamide, BCB (benzocyclobutene), etc., can be used. Here, acrylic of the type that, after applied to the substrate, thermally polymerizes was used; it was fired at 250°C, whereby the second interlayer insulating film was formed. (Fig. 11B)

A capacitor for a D/A converter circuit is then formed here. An electrode which should function as the electrode of the capacitor of the D/A converter circuit is formed from the same wiring layer as the drain wiring. All of the second interlayer insulating film 6055 is removed in the areas above the electrode. (Not shown) A black matrix is then formed. (Not shown) In this embodiment the black matrix is a laminate structure formed from a Ti film of 100 nm and an alloy film of Al and Ti with a thickness 300 nm. Accordingly a capacitor of the D/A converter circuit is formed in this embodiment between the electrode and the black matrix.

Thereafter a third interlayer insulating film 6059 is formed from an organic resin into 1.0 to 1.5 μm. As the organic resin, similar resins as the second interlayer insulating film may be used. Here a polyimide of a type that thermally polymerizes after application to the substrate is used and the film is formed by firing at 300 °C.

Then, a contact hole reaching the drain wiring 6053 is formed in the second interlayer insulating film 6055 and the third interlayer insulating film 6059, and a pixel electrode 6060 is formed. In forming a transmission type liquid crystal panel of the present invention, a transparent conductive film of ITO or the like is used as the pixel electrode 6060. (Fig. 11B)

In this way, a substrate having the TFTs of the driver circuit and the pixel TFTs of the pixel section on the same substrate can be completed. In the driver circuit, there are formed a P-channel TFT 6101, a first N-channel TFT 6102 and a second N-channel TFT 6103, while, in the pixel portion, there are formed a pixel TFT 6104 and a storage capacitor 6105. (Fig. 12) In this specification, such a substrate is called active matrix substrate for convenience.

Next the processes for forming a transmission type liquid crystal panel from an active matrix substrate manufactured through the above processes is described.

An alignment film 6061 is formed on the active matrix substrate of the state of Fig. 12. Polyimide is used as the alignment film 6061 in the present embodiment. An opposing substrate is next prepared. The opposing substrate comprises a glass substrate 6062, an opposing electrode 6063 comprising a transparent conductive film and an alignment film 6064.

Note that in the present embodiment a polyimide film of the type in which liquid crystal molecules are oriented in parallel with respect to the substrate is used as the alignment film. By performing rubbing treatment after forming the alignment film, liquid crystal molecules are made to orient in parallel with a prescribed pre-tilt angle.

Next the active matrix substrate which went through the above processes and the opposing substrate are stuck together through a sealant, spacers (neither shown) or the like by a known cell assembly process. Thereafter liquid crystal 6065 is injected between the both substrates and completely sealed with a sealant (not shown). A transmission type liquid crystal panel as shown in Fig. 12 is thus completed.

Note that in the present embodiment the transmission type liquid crystal panel is made to perform display by a TN (twist) mode. Therefore the a polarizing plate (not shown) is disposed on the transmission type liquid crystal panel.

The P-channel TFT 6101 in the driver circuit has a channel-forming region 806, source regions 807a and 807b and drain regions 808a and 808b in the island semiconductor layer 6004. The first N-channel TFT 6102 has a channel-forming region 809, an LDD region 810 overlapping the gate electrode 6071 (such an LDD region will hereinafter be referred to as Lov), a source region 811 and a drain region 812 in the island semiconductor layer 6005. The length in the channel direction of this Lov region is set to 0.5 to 3.0 μm, preferably 1.0 to 1.5 μm. A second N-channel TFT 6103 has a channel-forming region 813, LDD regions 814 and 815, a source region 816 and a drain region 817 in the island semiconductor layer 6006. In these LDD regions, there are formed Lov regions and LDD regions which do not overlap the gate electrode 6072(such an LDD region will hereafter be referred as Loff); and the length in the channel direction of this Loff region is 0.3 to 2.0 μm, preferably 0.5 to 1.5 μm. The pixel TFT 6104 has channel-forming regions 818 and 819, Loff regions 820 to 823, and source or drain regions 824 to 826 in the island semiconductor layer 6007. The length in the channel direction of the Loff regions is 0.5 to 3.0 μm, preferably 1.5 to 2.5 μm. In addition, offset regions (not shown) are formed between the channel forming regions 818 and 819 of the pixel TFT 6104 and Loff regions 820 to 823 that are LDD regions of the pixel TFT. Further, the storage capacitor 6105 comprises capacitor wiring 6074, an insulating film composed of the same material as the gate insulating film 6020 and a semiconductor layer 827 which is connected to the drain region 826 of the pixel TFT 6104 and in which an impurity element for imparting the n conductivity type is added. In Fig. 12, the pixel TFT 6104 is of the double gate structure, but may be of the single gate structure, or may be of a multi-gate structure in which a plurality of gate electrodes are provided.

As described above, the TFT structures that constitute each circuit are optimized in accordance with the specifications required by the pixel TFT and the driver, and it is possible to improve the operation performance and reliability of the liquid crystal panel.

A transmission type liquid crystal panel is described in this embodiment. However, liquid crystal panels of the present invention is not limited to this type, and may be applied also to a reflection type liquid crystal panel.

[Embodiment 2]

Various liquid crystals other than the nematic liquid crystal may be used for the above liquid crystal panel of the liquid crystal display device of the present invention. For instance, usable liquid crystals are the ones disclosed in: "Characteristics and Driving Scheme of Polymer-Stabilized Monostable FLCD Exhibiting Fast Response Time and High Contrast Ratio with Gray-Scale Capability" by H. Furue et al.; 1997, SID DIGEST, 841, "A Full-Color Thresholdless Antiferroelectric LCD Exhibiting Wide Viewing Angle with Fast Response Time" by T. Yoshida et al.; 1996, J. Mater. Chem. 6(4), 671-673, "Thresholdless antiferroelectricity in liquid crystals and its application to displays" by S. Inui et al.; and US Patent No. 5,594,569.

Fig. 13 shows an electro optical characteristic of a monostable FLC (ferroelectric liquid crystal) obtained by employing an FLC that exhibits a transition series of isotropic phase - cholesteric phase - chiral smectic C phase, causing cholesteric phase - chiral smectic C phase transition with DC voltage applied to the FLC, and making the cone edge almost coincide with the rubbing direction. The display mode of ferroelectric liquid crystals having a characteristic as shown in Fig. 13 is called "Half-V shape switching mode". The axis of ordinate of the graph shown in Fig. 13 indicates transmittance (arbitrary unit), and the axis of abscissa indicates applied voltage. Details of the "Half-V shape switching mode" is discussed in "Half-V shape Switching

Mode FLCD", Terada et al., Extended Abstracts of the 46th Convention of The Japan Society of Applied Physics, p. 1316, March 1999, and "Time-division Full Color LCD Using Ferroelectric Liquid Crystal", Yoshihara et al., Liquid Crystal Vol. 3, No. 3, p. 190.

As shown in Fig. 13, using such a ferroelectric mixed liquid crystal allows liquid crystal panels to be driven at a low voltage and to display on gray-scale basis. The ferroelectric liquid crystals showing the electro optical characteristic as such may also be used for the liquid crystal panel of the liquid crystal display device according to the present invention.

Liquid crystals exhibiting antiferroelectric phase in a certain temperature range are called antiferroelectric liquid crystals (AFLC). Among mixed liquid crystals having antiferroelectric liquid crystals, there are ones called thresholdless antiferroelectric mixed liquid crystals showing an electro optical response characteristic in which transmittance continuously changes in relation to the electric field. Some thresholdless antiferroelectric liquid crystals show an electro optical response characteristic of so-called V shape type, and there have been found ones whose drive voltage is about ± 2.5 V (cell thickness thereof is about 1 μm to 2 μm).

In thresholdless antiferroelectric mixed liquid crystals, generally, spontaneous polarization is large and the dielectric constant of the liquid crystals themselves is high. For this reason, a relatively large storage capacitor is needed for a pixel when thresholdless antiferroelectric mixed liquid crystals are used for liquid crystal display devices. It is thus preferable to employ a thresholdless antiferroelectric mixed liquid crystal whose spontaneous polarization is small.

To use such a thresholdless antiferroelectric mixed liquid crystal for the liquid crystal display device of the present invention realizes low voltage driving, simultaneously realizing power consumption reduction.

[Embodiment 3]

Display devices of the present invention can be used by incorporating them into various electronic equipment.

Examples of the electronic equipment include a video camera, a digital camera, a projector (rear type or front type), a head mounted display (a goggle type display), a game machine, a car navigation system, a personal computer and a portable information terminal (a mobile computer, a cellular telephone, an electronic book, etc.). Figs. 14A and 14B, and Figs15A to 15F show some examples of them.

Fig. 14A shows the front type projector comprising a main body 10001, a liquid crystal display 10002 of the present invention, a light source 10003, an optical system 10004, and a screen 10005. It is noted that although Fig. 14A shows the front projector in which one liquid crystal display is built in, a front type projector of higher resolution and higher definition can be realized by combining three liquid crystal display devices (corresponding to light of R, G and B, respectively).

Fig. 14B shows the rear type projector comprising a main body 10006, a liquid crystal display device 10007 of the present invention, a light source 10008, a reflector 10009 and a screen 10010. Fig. 14B shows a rear projector in which three liquid crystal displays are built in (corresponding to light of R, G and B, respectively). Further, the rear type projector in which one liquid crystal display is built in can be provided.

Fig. 15A shows a personal computer, which comprises: a main body 7001; an image input section 7002; a liquid display device of the present invention 7003; and a keyboard 7004.

Fig. 15B shows a video camera, which comprises: a main body 7101; a liquid display device of the present invention 7102; a sound input section 7103; an operation switch 7104; a

battery 7105; and an image receiving section 7106.

Fig. 15C shows a mobile computer, which comprises: a main body 7201; a camera section 7202; an image receiving section 7203; an operation switch 7204; and a display device of the present invention 7205.

Fig. 15D shows a goggle type display, which comprises: a main body 7301; a liquid display device of the present invention 7302; and an arm section 7303.

Fig. 15E shows a player employing a recording medium storing a program (hereinafter called the recording medium). It comprises a main body 7401, a liquid display device of the present invention 7402, a speaker unit 7403, a recording medium 7404 and an operation switch 7405. Note that by using DVD (digital versatile disc), CD, etc. as a recording medium of this device, music appreciation, film appreciation, games or the use for Internet can be performed.

Fig. 15F shows a display device using a liquid crystal display device of the present invention. It comprises a main body 7501 and a liquid crystal display device of the present invention 7502.

As described above, the applicable range of the present invention is very large, and it can be applied to electronic equipment of various fields.

The present invention is applied to not only a liquid crystal display device another devices such as an EL display device. According to the present invention, a display device with a small size liquid crystal panel can be obtained even when the area a source drive occupies is large.

WHAT IS CLAIMED IS:

1. A display device comprising:

a pixel portion including **m** x **n** pixels (**m** and **n** are both natural numbers and satisfy the relation **m** < **n**), said pixels each having a TFT;

a gate driver for feeding **n** gate signal lines with selection signals;

a source driver for feeding **m** source signal lines with video data; and

a video data converter circuit, wherein

said video data converter circuit converts first video data (**h**, **k**) (**h** = 1 ~ **m**, **k** = 1 ~ **n**) into second video data, and wherein

the video data (**h**, **k**) constituting said first video data is converted into {**m**(**k** - 1) + **h**}-th video data that constitutes said second video data.

2. A display device comprising:

a pixel portion including **m** x **n** pixels (in a pixel (**h**, **k**),**h** = 1 ~ **m**, **k** = 1 ~ **n**, with **m** and **n** both being natural numbers and satisfying the relation **m** < **n**), said pixels each having a TFT;

a gate driver for feeding **n** gate signal lines with selection signals;

a source driver for feeding **m** source signal lines with video data; and

a video data converter circuit, wherein

said video data converter circuit converts first video data (**h**, **k**) (**h** = 1 ~ **m**, **k** = 1 ~ **n**) which is to be fed to said pixel (**h**, **k**) into second video data, and wherein

the video data (**h**, **k**) constituting said first video data is converted into {**m**(**k** - 1) + **h**}-th video data that constitutes said second video data.

3. A rear projector wherein three display devices according to claim 1 are used.

4. A front projector wherein three display devices according to claim 1 are used.

5. A rear projector wherein one display device according to claim 1 is used.

6. A front projector wherein one display device according to claim 1 is used.

7. Electronic equipment comprising a display device according to claim 1 is selected from the group consisting of a head mount display, a computer, a video camera, a DVD player, and display apparatus.

8. A rear projector wherein three display devices according to claim 2 are used.

9. A front projector wherein three display devices according to claim 2 are used.

10. A rear projector wherein one display device according to claim 2 is used.

11. A front projector wherein one display device according to claim 2 is used.

12. Electronic equipment comprising a display device according to claim 2 is selected from the group consisting of a head mount display, a computer, a video camera, a DVD player, and display apparatus.

13. A display device according to claim 1 is a liquid crystal display device.

14. A display device according to claim 2 is a liquid crystal display device.

15. A display device comprising:

a pixel portion including **m** x **n** pixels (**m** and **n** are both natural numbers and satisfy the relation **m** < **n**), said pixels each having a TFT;

a gate driver for feeding **n** gate signal lines with selection signals; and

a source driver for feeding **m** source signal lines with video data.

16. Electronic equipment comprising a display device according to claim 15 is selected from the group consisting of a front projector, a rear projector, a head mount display, a computer, a video camera, a DVD player, and display apparatus.

17. A display device according to claim 15 is a liquid crystal display device.

18. A display device comprising:

a pixel portion including a plurality of pixels each having a TFT;

a gate driver provided above said pixel portion; and

a source driver provided on one side of said pixel portion,

wherein a lateral length of said pixel portion is longer than a longitudinal length.

19. Electronic equipment comprising a display device according to claim 18 is selected from the group consisting of a front projector, a rear projector, a head mount display, a computer, a video camera, a DVD player, and display apparatus.

20. A display device according to claim 18 is a liquid crystal display device.

21. A display device comprising:

a pixel portion including a plurality of pixels each having a TFT;

a plurality of gate signal lines connected to a gate driver; and

a plurality of source signal lines connected to a source driver,

wherein said plurality of gate signal lines are vertical and said plurality of source signal lines are horizontal.

22. Electronic equipment comprising a display device according to claim 21 is selected from the group consisting of a front projector, a rear projector, a head mount display, a computer, a video camera, a DVD player, and display apparatus.

23. A display device according to claim 21 is a liquid crystal display device.

ABSTRACT OF THE DISCLOSURE

To provide a liquid crystal panel employing a circuit layout that makes it possible to obtain a small size liquid crystal panel when the area a source driver occupies is large. A liquid crystal display device of the present invention comprises: a pixel portion including **m** x **n** pixels (**m** and **n** are both natural numbers and satisfy the relation **m** < **n**), the pixels each having a TFT; a gate driver for feeding **n** gate signal lines with selection signals; a source driver for feeding **m** source signal lines with video data; and a video data converter circuit, and is characterized in that the video data converter circuit converts first video data (**h**, **k**) (**h** = 1 ~ **m**, **k** = 1 ~ **n**) into second video data, and in that the video data (**h**, **k**) constituting the first video data is converted into {**m**(**k** - 1) + **h**}-th video data that constitutes the second video data.

Fig.1

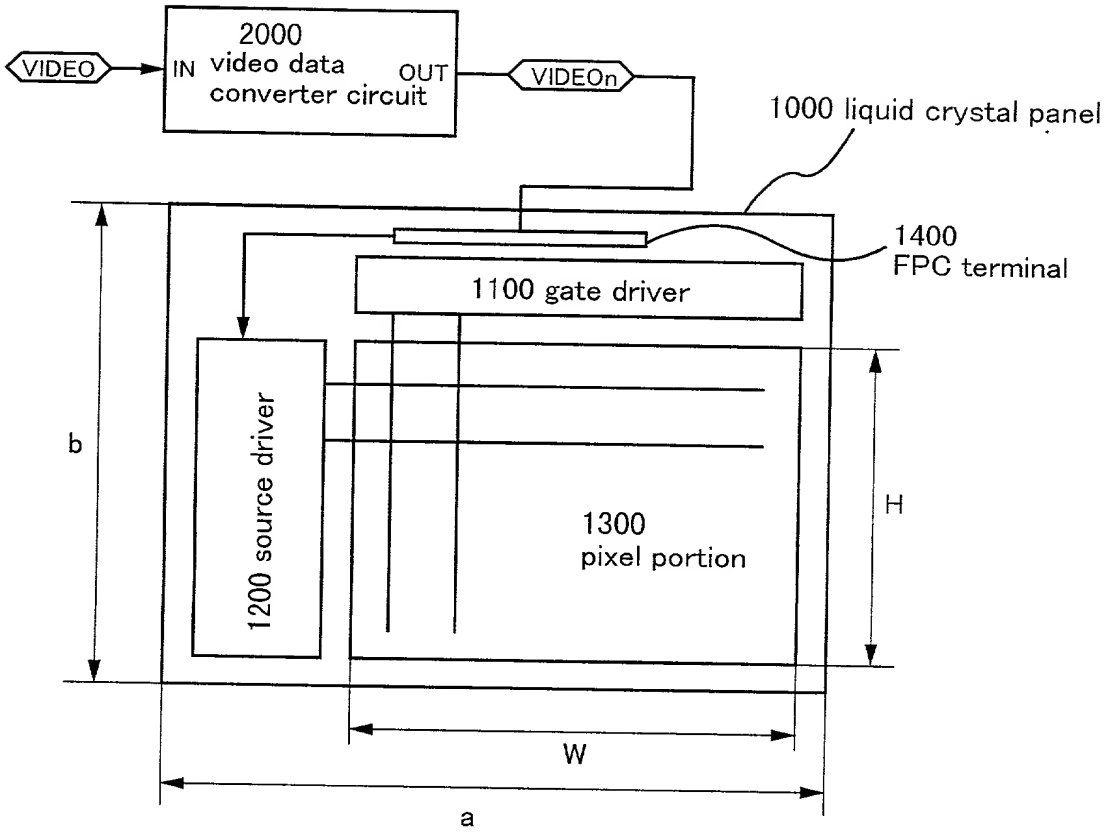
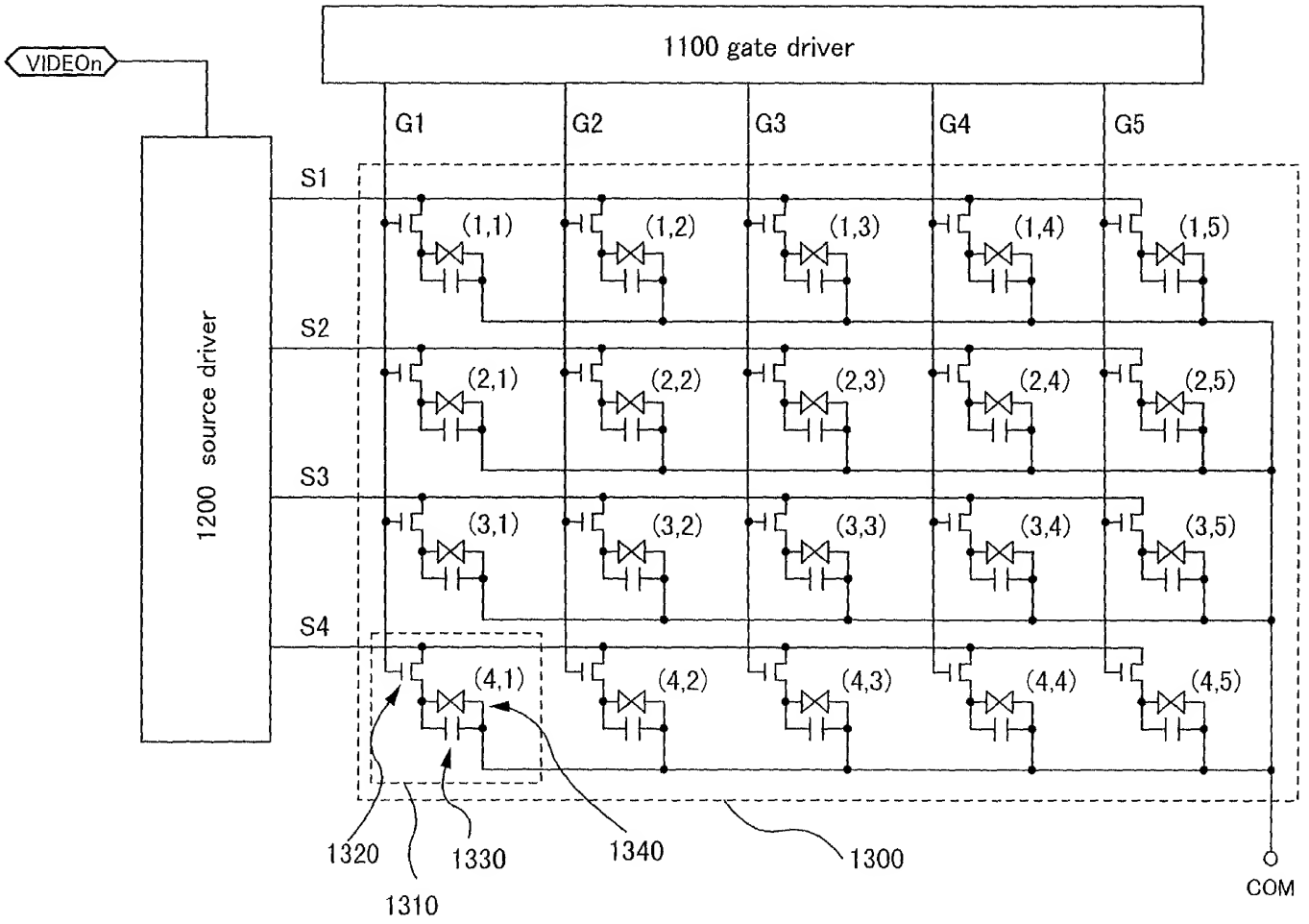

VIDEO
IN
2000
video data
converter circuit
OUT
VIDEOn
1000 liquid crystal panel
1400
FPC terminal
1100 gate driver
1200 source driver
1300
pixel portion
b
H
W
a

Fig.2


VIDEOn
1100 gate driver
1200 source driver
G1
G2
G3
G4
G5
S1
S2
S3
S4
(1,1)
(1,2)
(1,3)
(1,4)
(1,5)
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(2,2)
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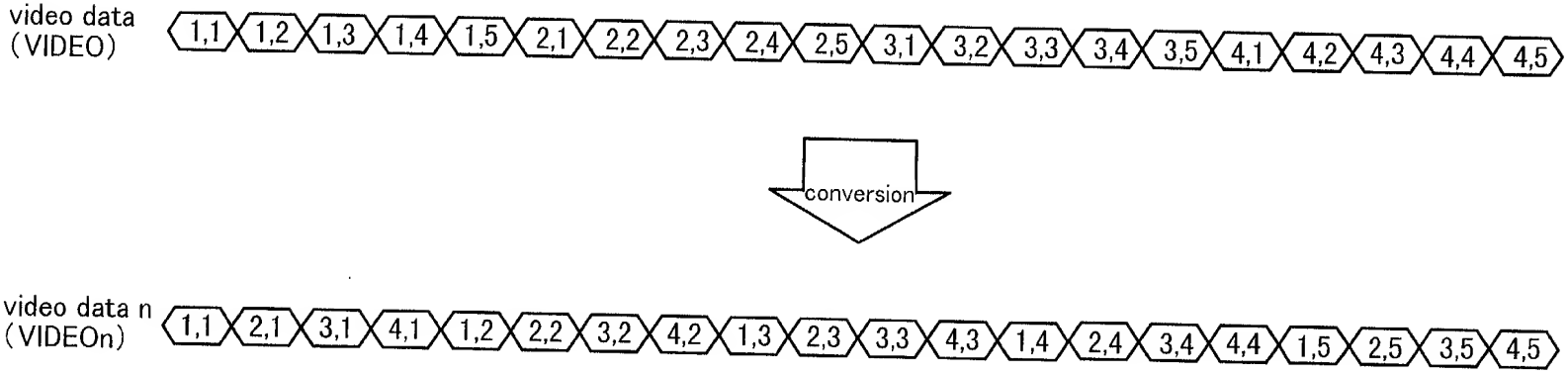
1320
1330
1340
1300
1310
COM

Fig.3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1,4
1,5
2,1
2,2
2,3
2,4
2,5
3,1
3,2
3,3
3,4
3,5
4,1
4,2
4,3
4,4
4,5
conversion
video data n
(VIDEOn)
1,1
2,1
3,1
4,1
1,2
2,2
3,2
4,2
1,3
2,3
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4,4
1,5
2,5
3,5
4,5

Fig.4

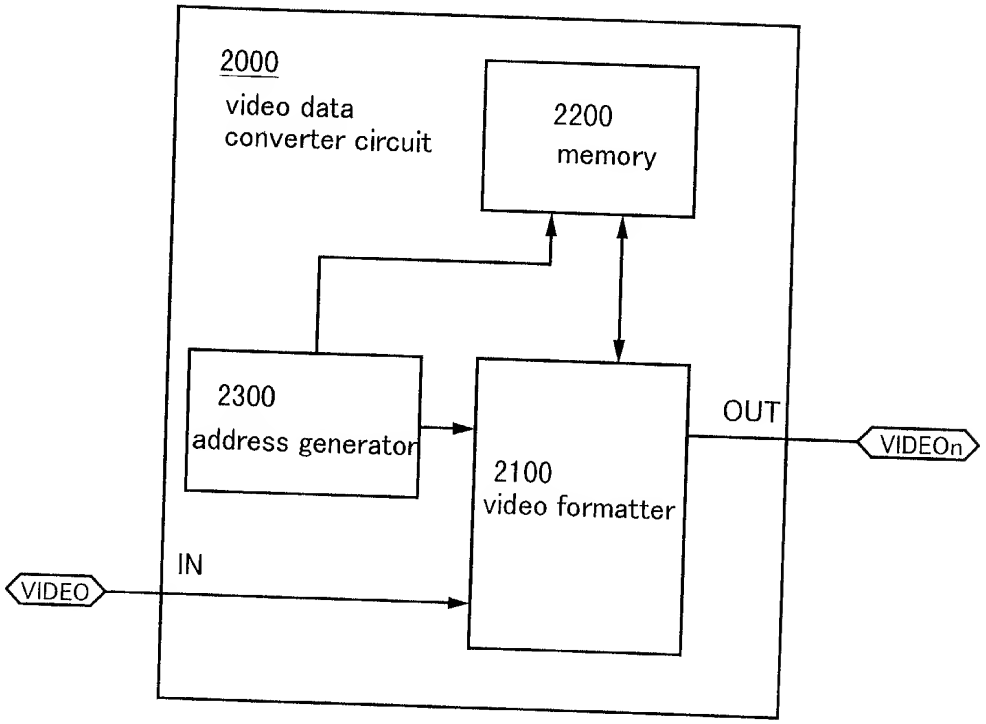
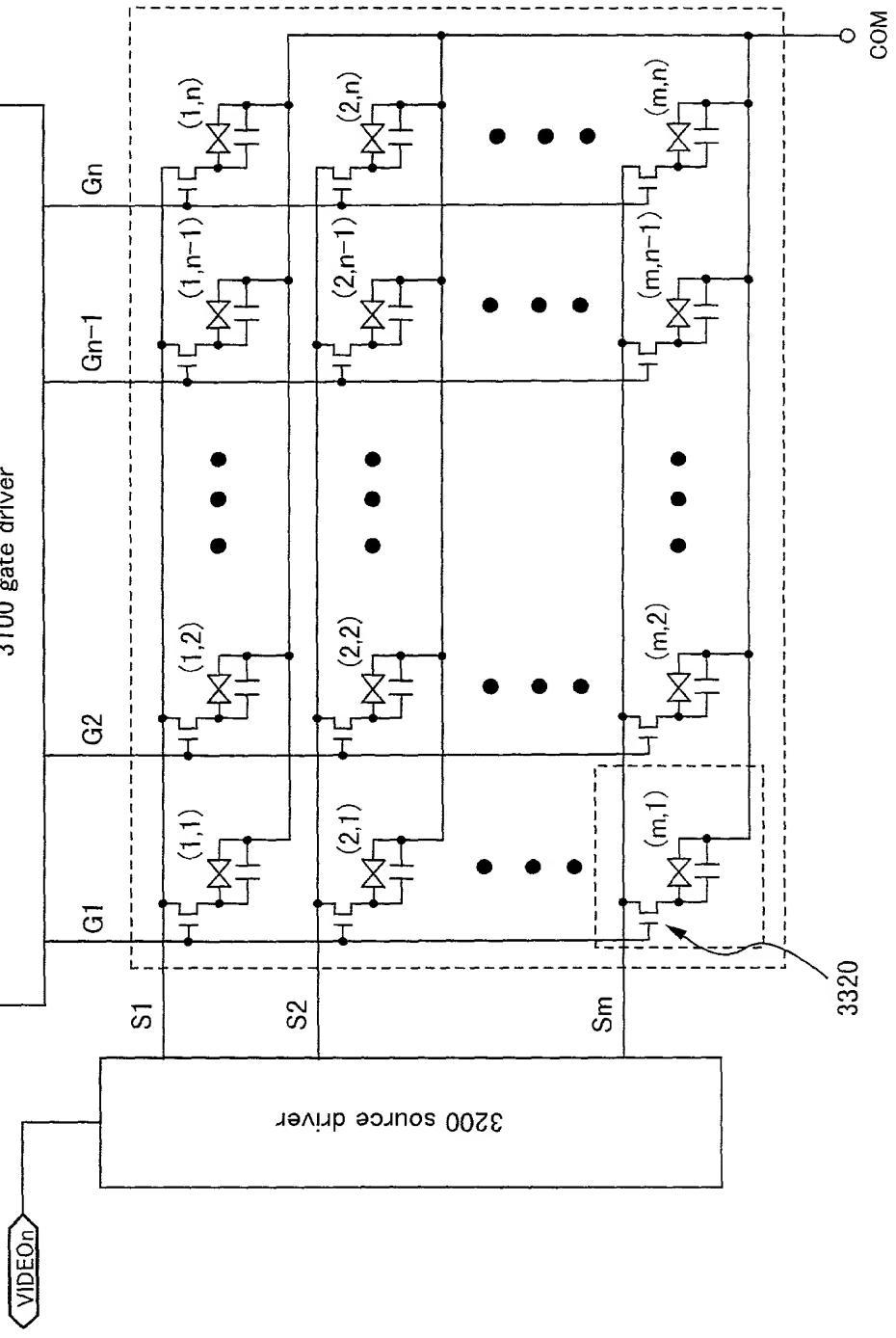

2000
video data
converter circuit
2200
memory
2300
address generator
2100
video formatter
OUT
VIDEOn
IN
VIDEO

Fig.5


VIDEOn
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3100 gate driver
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S2
Sm
G1
G2
Gn-1
Gn
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(1,2)
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(2,1)
(2,2)
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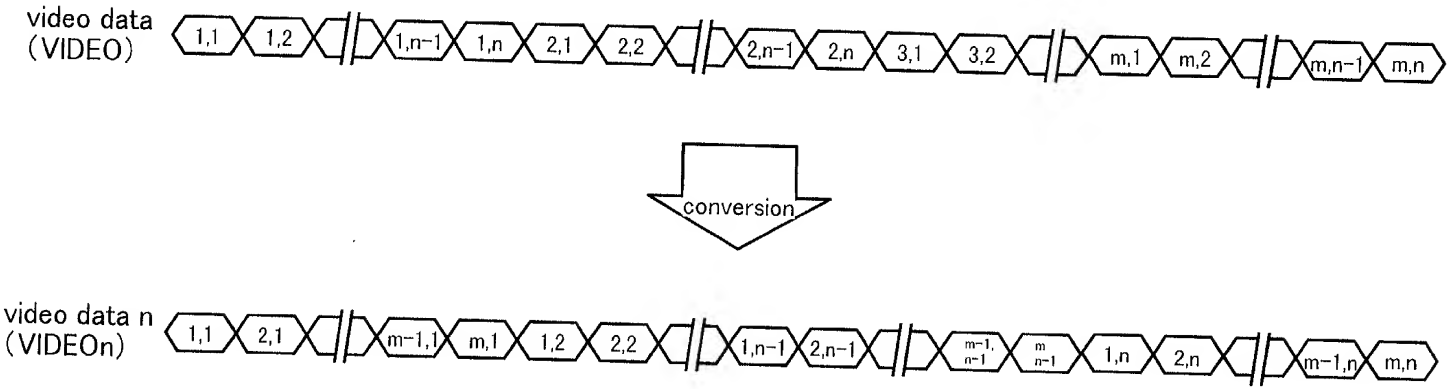
(m,n)
3320
COM

Fig.6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1,2
1,n-1
1,n
2,1
2,2
2,n-1
2,n
3,1
3,2
m,1
m,2
m,n-1
m,n
conversion
video data n
(VIDEOn)
1,1
2,1
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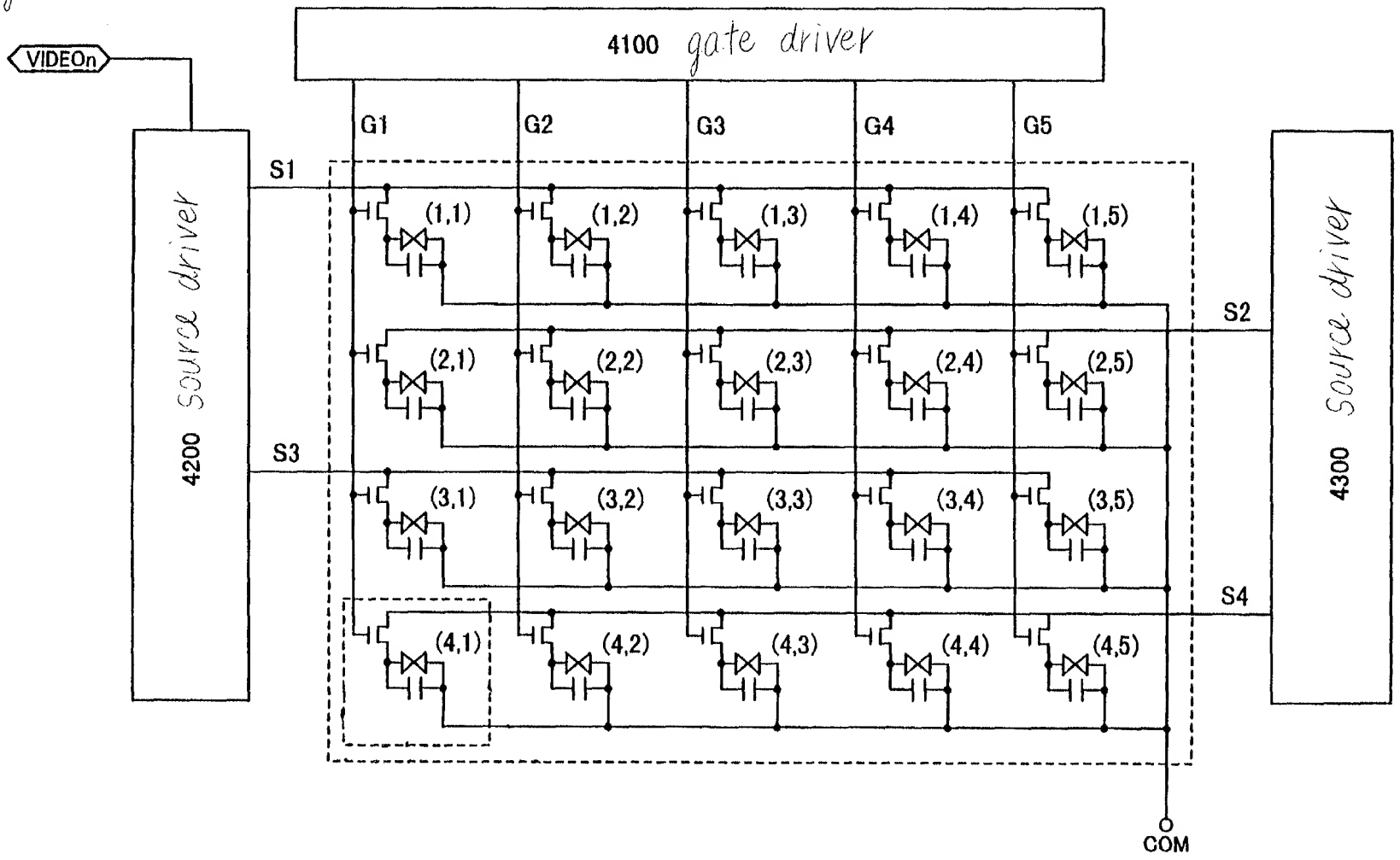
m,1
1,2
2,2
1,n-1
2,n-1
m-1,
n-1
m
n-1
1,n
2,n
m-1,n
m,n

Fig. 7


4100 gate driver
VIDEOn
4200 source driver
4300 source driver
G1
G2
G3
G4
G5
S1
S2
S3
S4
(1,1)
(1,2)
(1,3)
(1,4)
(1,5)
(2,1)
(2,2)
(2,3)
(2,4)
(2,5)
(3,1)
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(4,4)
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COM

Fig.8A

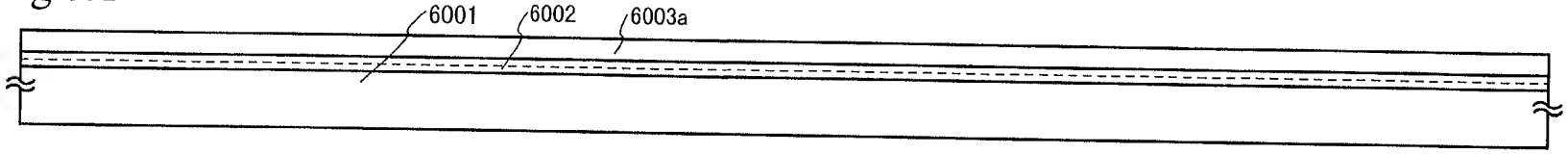


Fig.8B

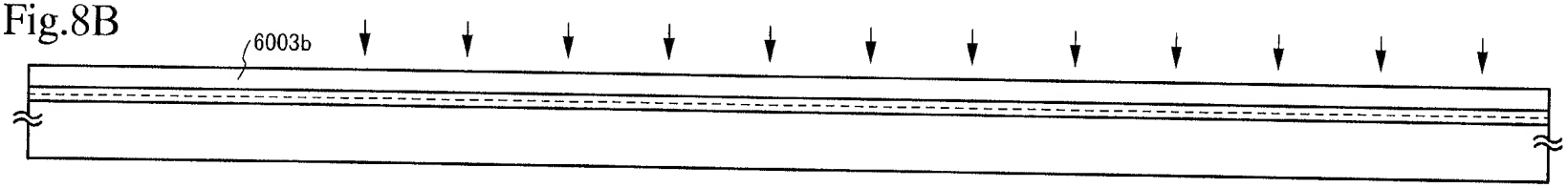


Fig.8C

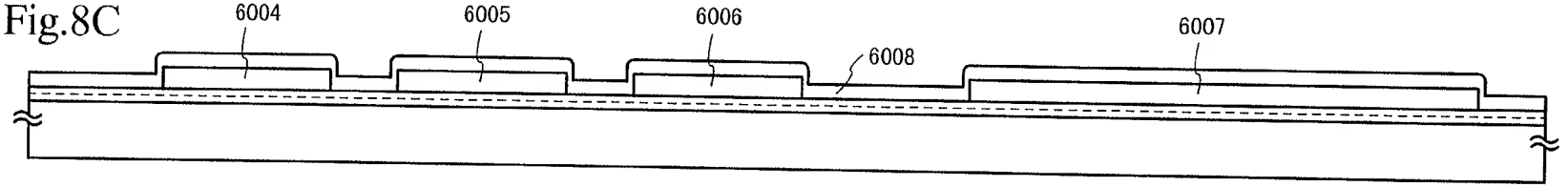


Fig.8D

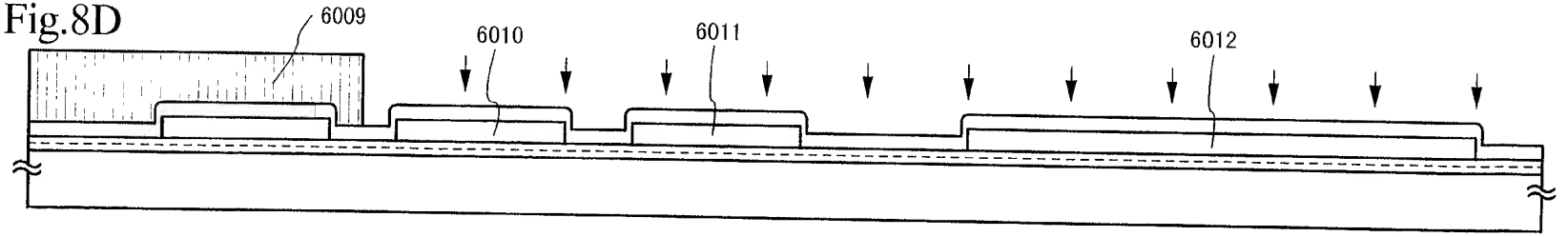


Fig.9A

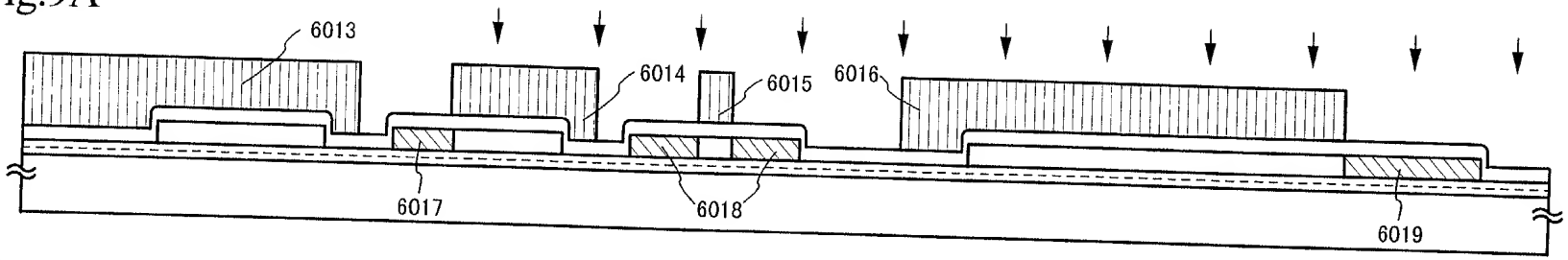


Fig.9B

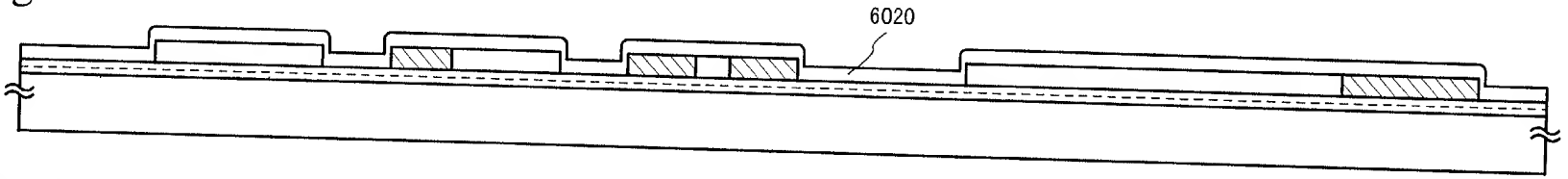


Fig.9C

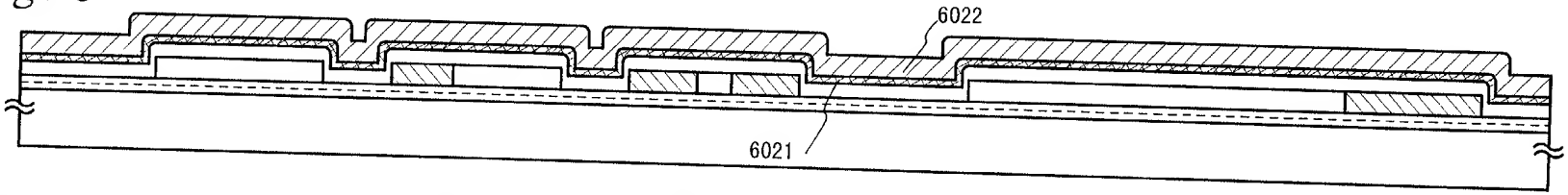


Fig.9D

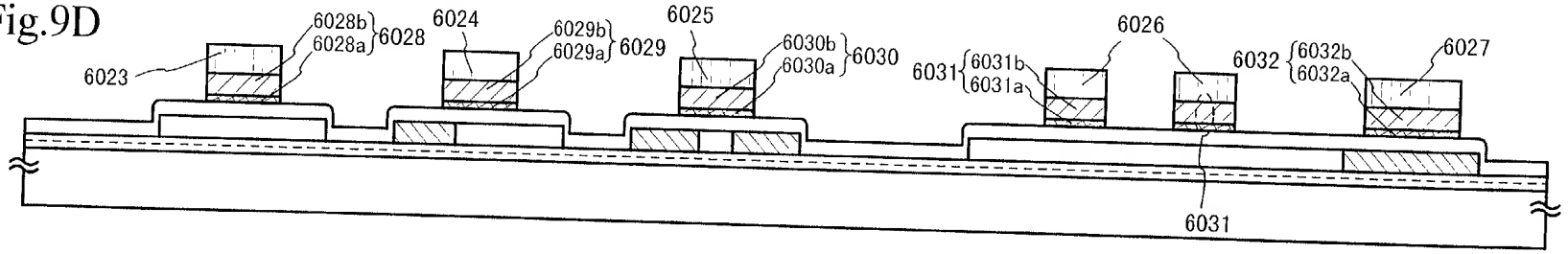


Fig.10A

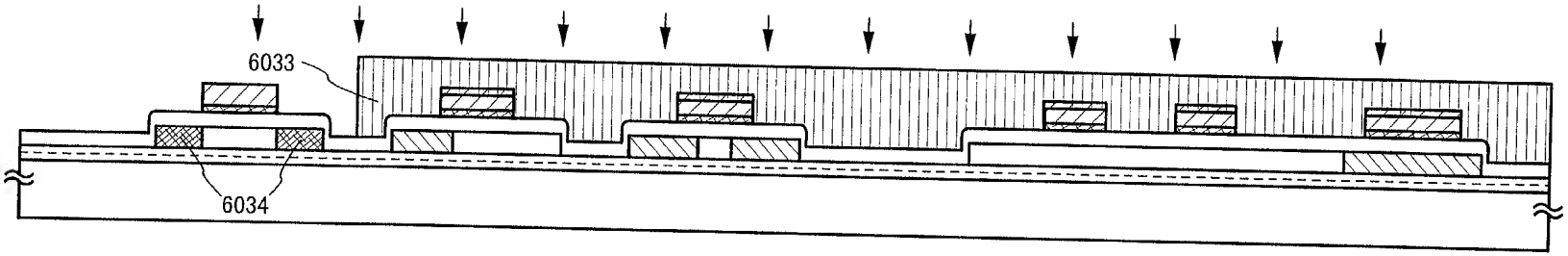


Fig.10B

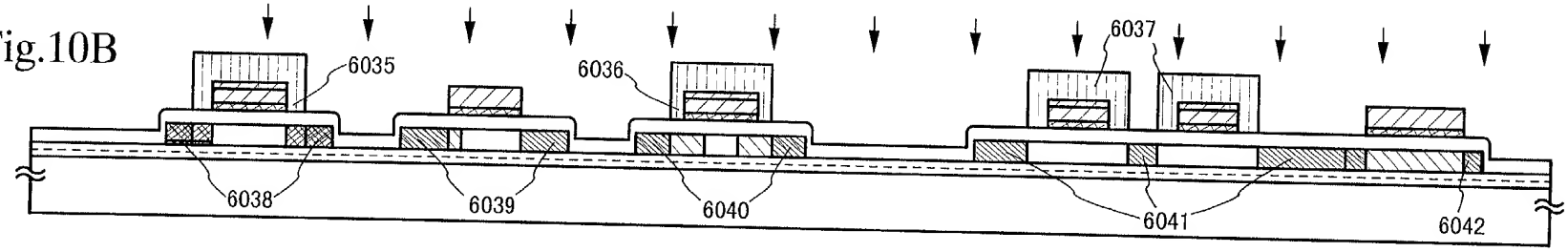


Fig.10C

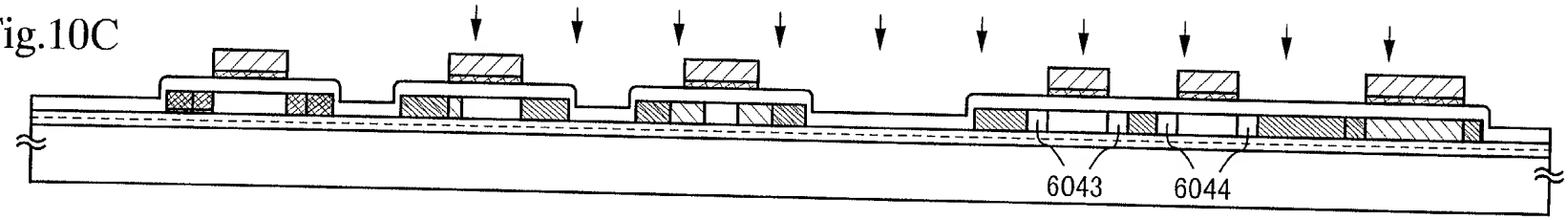


Fig.10D

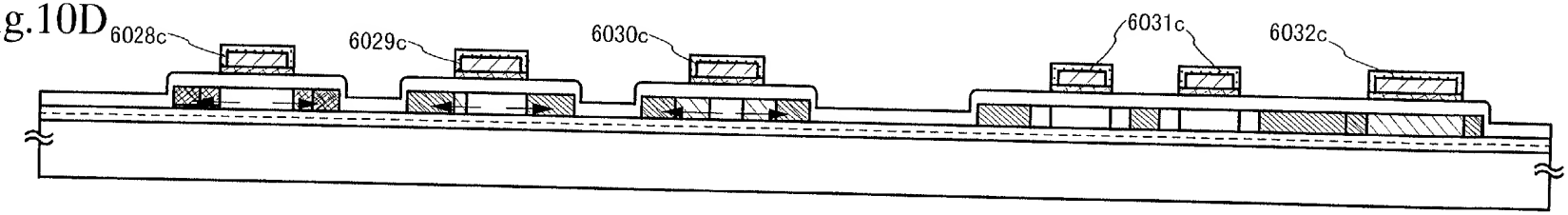


Fig.11A

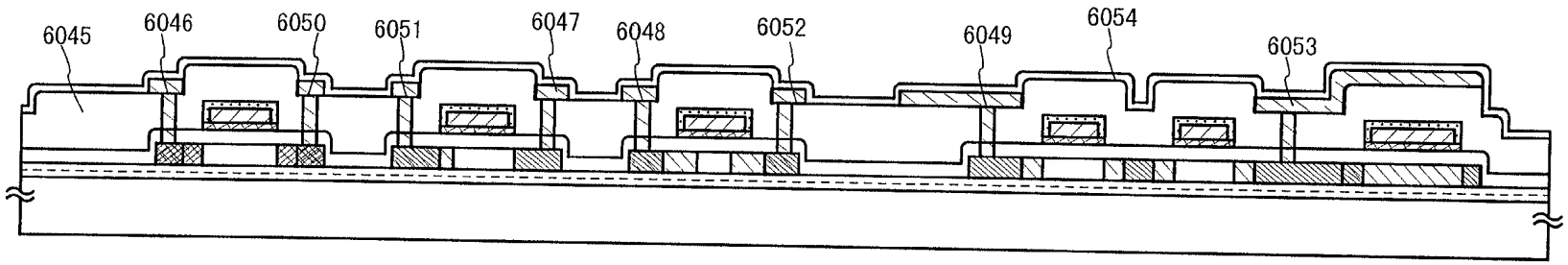


Fig.11B

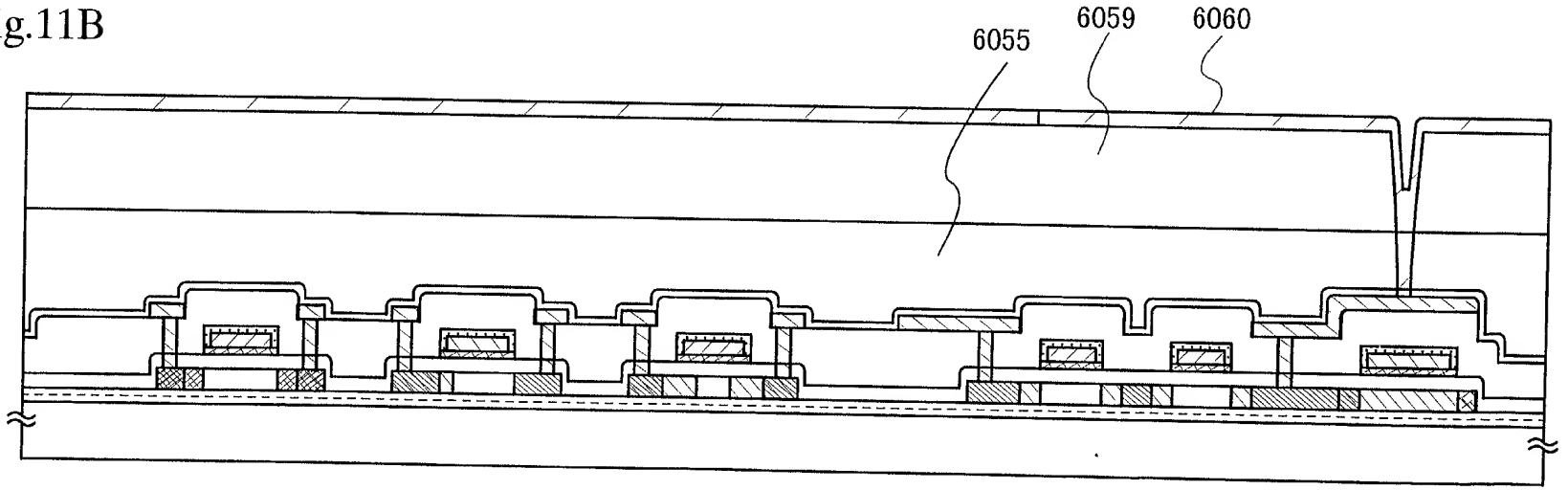
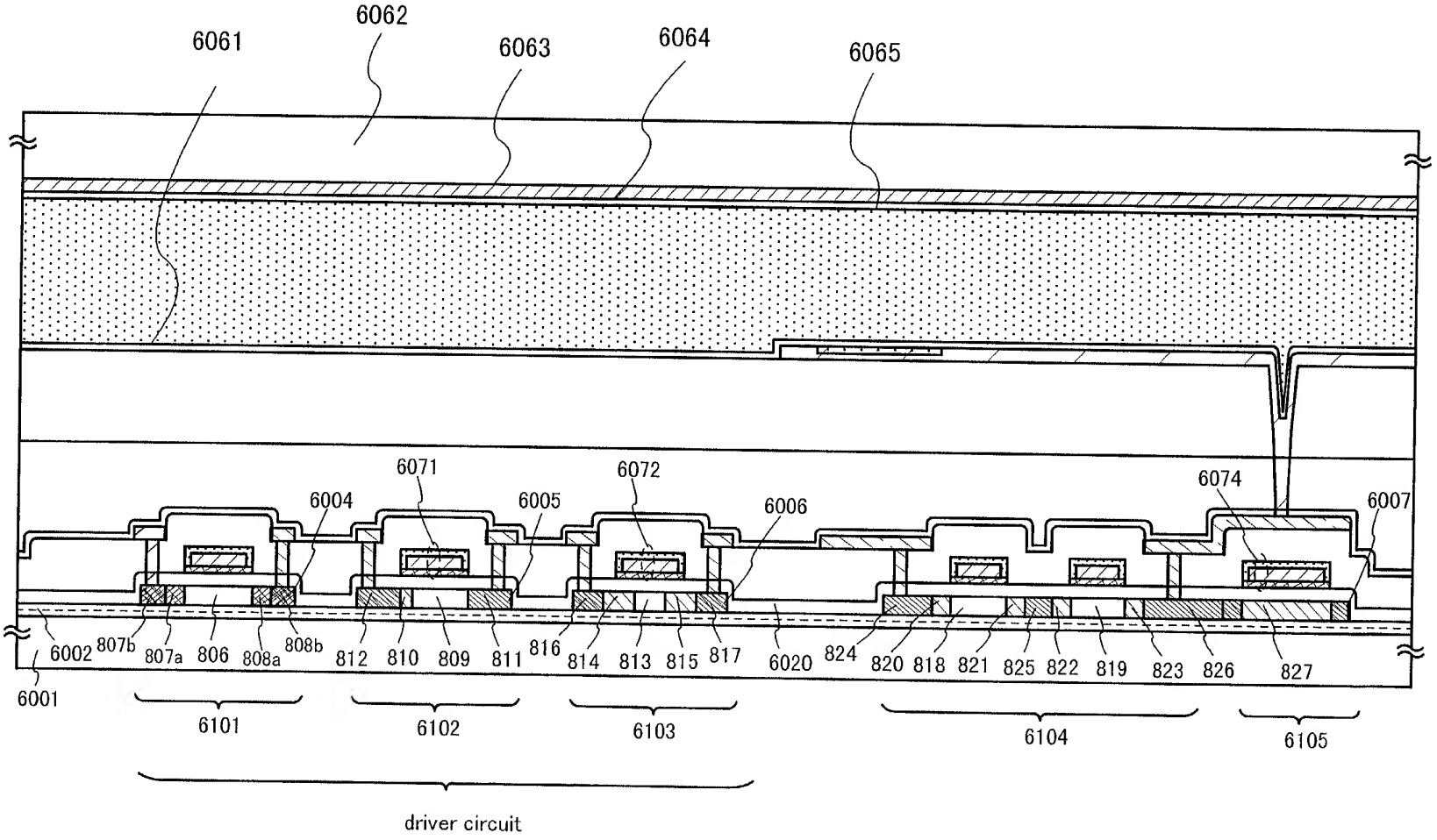


Fig.12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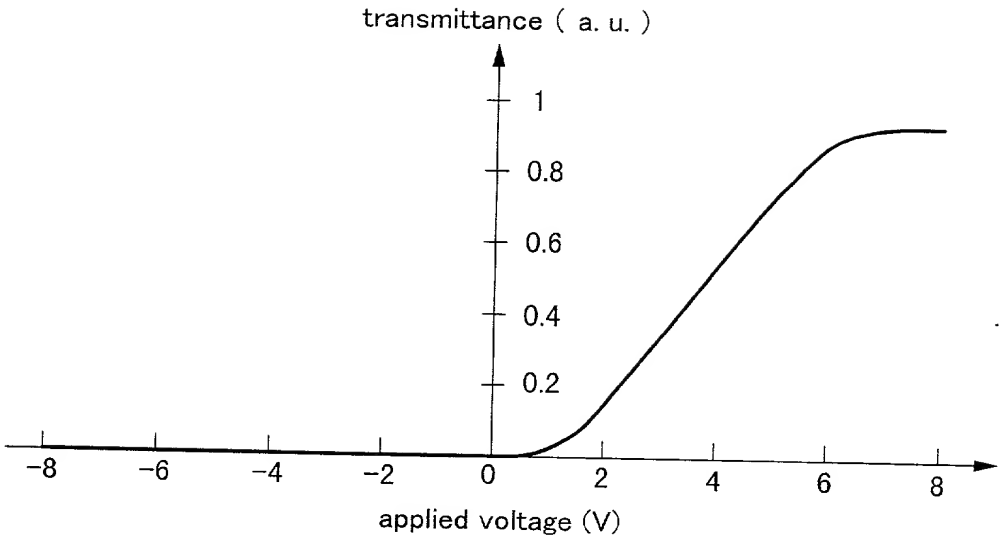
6101
6102
6103
6104
6105
driver circuit

Fig.13



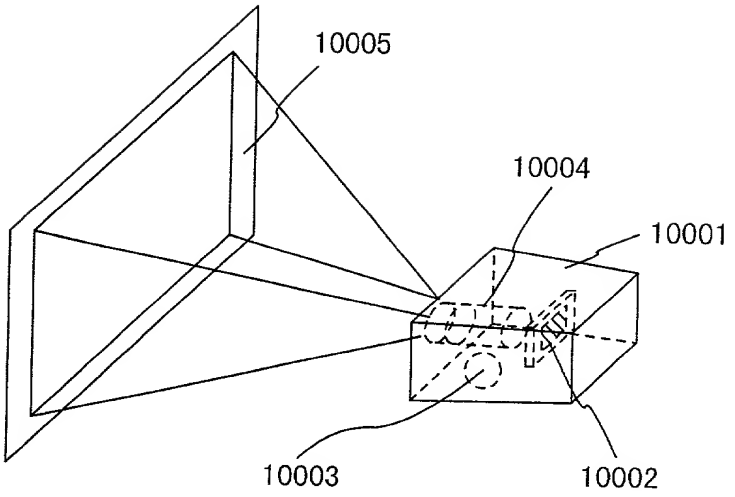


Fig.14A

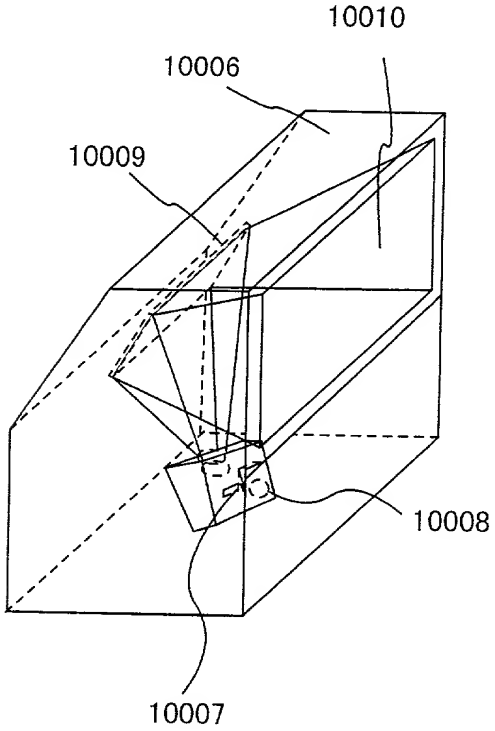


Fig.14B

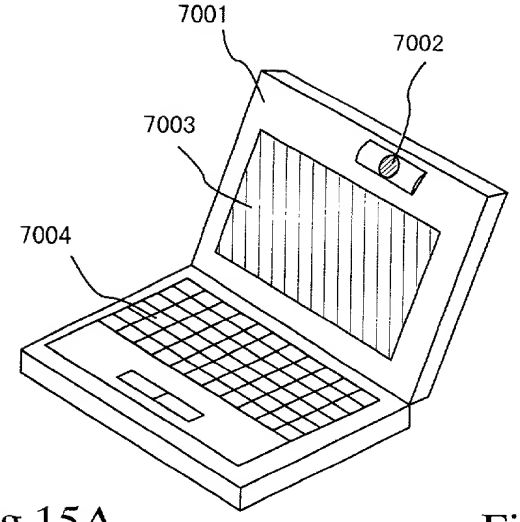


Fig.15A

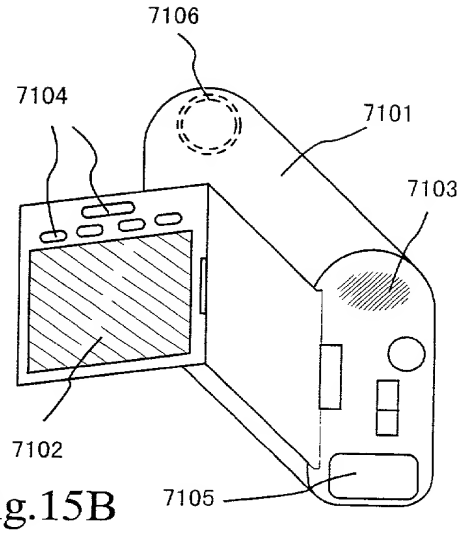


Fig.15B

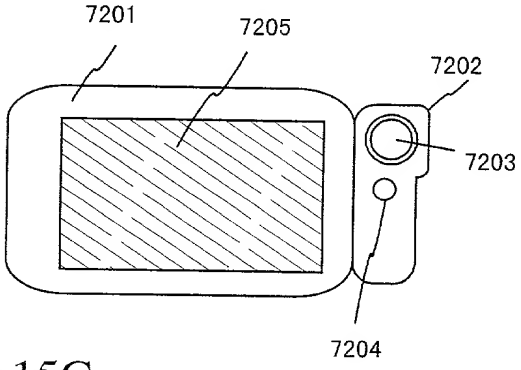


Fig.15C

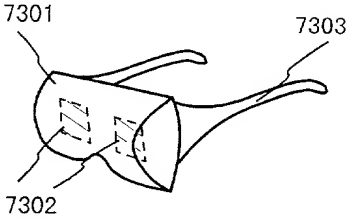


Fig.15D

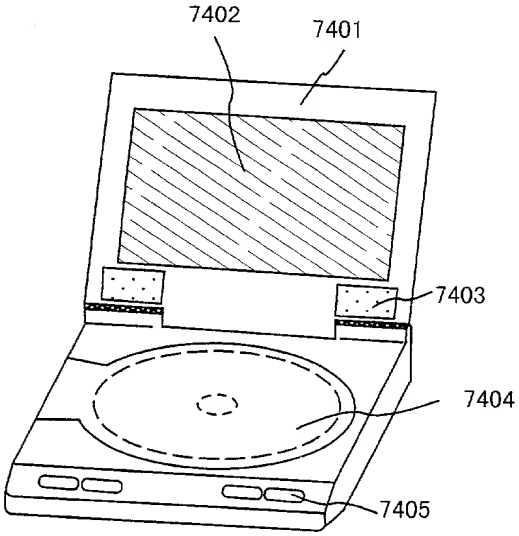


Fig.15E

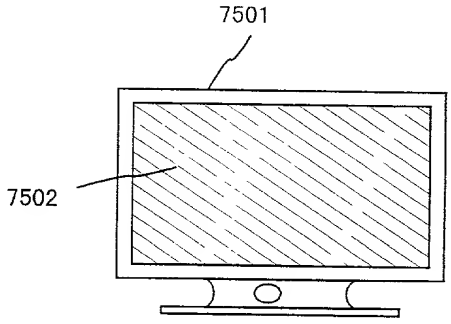
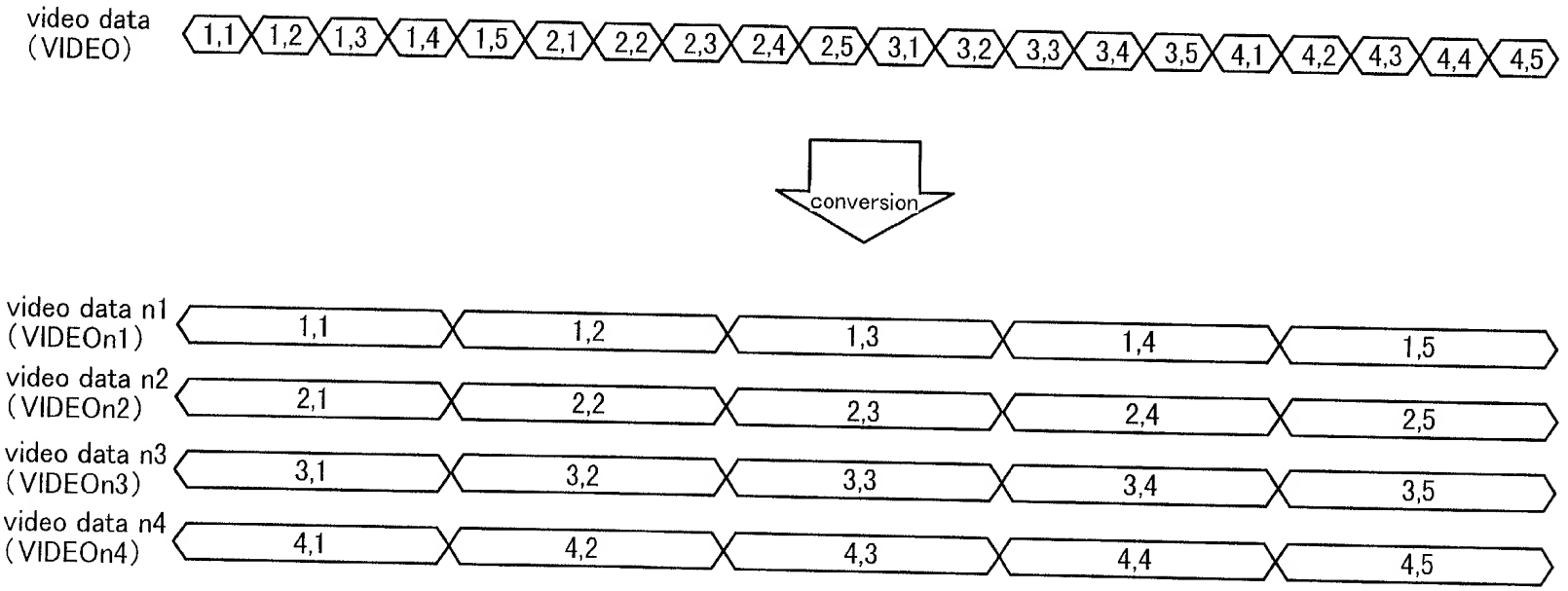


Fig.15F

Fig.16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4,5
conversion
video data n1
(VIDEOn1)
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1,4
1,5
video data n2
(VIDEOn2)
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video data n3
(VIDEOn3)
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video data n4
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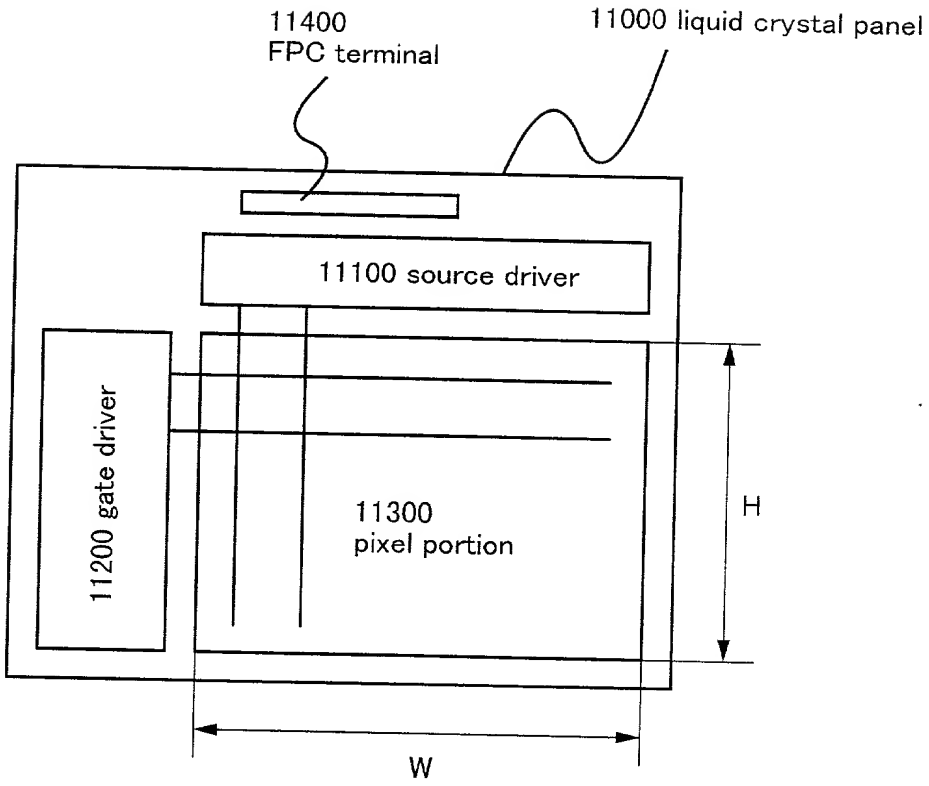
4,2
4,3
4,4
4,5

Fig.17


11400
FPC terminal
11000 liquid crystal panel
11100 source driver
11200 gate driver
11300
pixel portion
H
W

Declaration and Power of Attorney For Patent Application
特許出願宣言書及び委任状

Japanese Language Declaration
日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

____

____

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DISPLAY DEVICE

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を __ __ __ __ __ __ とし、（該当する場合） __________に訂正されました。

☐ was filed on ______________ as United States Application Number or PCT International Application Number ______________ and was amended on ______________ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第 37 編第 1 条 56 項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第 35 編 119 条(a)-(d)項又は 365 条(b)項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約 365(a)項に基く国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			**Priority Not Claimed** 優先権主張なし
11-287583 (Number) (番号)	Japan (Country) (国名)	October 8, 1999 (Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

私は、第35編米国法典119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第35編120条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約 365 条(c)に基く権利をここに主張します。また、本出願の各請求範囲の内容が米国法典代 35 編 112 条第 1 項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規制法典第 37 編 1 条 56 項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、継続中、放棄済)

(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況： 特許許可済、継続中、放棄済）

私は、私自身の知識に基いて本宣言書中で私が行う表明が真実であり、かつ私の入手した情報と私の信じるところに基く表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第 18 編第 1001 条に基き、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁護士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number).

Edward D. Manzo (Reg. No. 28, 139)

ここに署名する者は、この申請に関して米国特許商標局においてなされるべき如何なる行動に関しても、ここに指名された米国弁護士または代理人が、米国弁護士または代理人とここに署名した者との間で直接の連絡を取ることなしに、_____からの指示を受け入れてそれに従う権限を与える。指示を出す人物に変更がある場合は、ここに指名された米国弁護士または代理人は、ここに署名した者からその旨通知を受ける。

The undersigned hereby authorizes any U. S. attorney or agent named herein to accept and follow instructions from _____ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U. S. attorneys or agents named herein will be so notified by the undersigned.

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(312) 236-8500

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発明者の署名　日付	Inventor's signature　Date Yukio Tanaka　10/02/2000
住所	Residence Kanagawa, Japan
国籍	Citizenship Japanese
私書箱	Post Office Address c/o Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan

Atty Docket SEL 219

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Yukio TANAKA

Serial No.: Not Assigned

Filed: Herewith

For: DISPLAY DEVICE

To:
Assistant Commissioner for Patents
Washington D.C. 20231

"Express Mail" Mailing Label No. EL613562765

Date of Deposit October 6, 2000

I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Washington, D.C. 20231

Name ARMANDO CHUNG
(typed or printed)

Signature Armando Chung

APPOINTMENT OF ASSOCIATE ATTORNEYS

Sir:

Please recognize the following as my associate attorneys in the above captioned application:

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Granger Cook, Jr.	Reg. No. 18,283
William H. Magidson	Reg. No. 19,902
John L. Alex	Reg. No. 22,017
Daniel M. Riess	Reg. No. 24,375
Eugene M. Cummings	Reg. No. 24,398
Raymond M. Mehler	Reg. No. 26,306
Gary W. McFarron	Reg. No. 27,357
Stephen B. Heller	Reg. No. 30,181
David Lesht	Reg. No. 30,472
Andrew G. Kolomayets	Reg. No. 33,723
Mark J. Murphy	Reg. No. 34,225
David M. Mundt	Reg. No. 41,207
John R. Lagowski	Reg. No. 41,922
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Respectfully submitted,

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